Reliability of Wide Bandgap Power Devices

Jerry L. Hudgins

Department of Electrical Engineering

UNIVERSITY OF NEBRASKA–LINCOLN

Power Electronics Applications Group

Electric Machines, Drives and Power Electronics Systems

Dr. Dean Patterson

Power Electronics, Controls, Distributed and Smart Power

Dr. Wei Qiao

Power Semiconductor Devices and Materials, Packaging, Power Electronics

Dr. Jerry Hudgins

Dr. Tanya Gachovska

Power Semiconductor Devices and Power Electronics

Dr. Liyan Qu

Electric Machines, FEM Analysis, Power Electronics

Dr. Yongfeng Lu

Laser Assisted Manufacturing and Carbon Nanotechnology

Device Failures

- Material defects are a root cause of device failures
  - These defects and corresponding secondary effects are exacerbated by additional energy from:
    - High Electric Fields
    - Large Current Densities
    - Increasing Temperature
    - Interface stress of material layers

- Non-micropipe defects in the bulk and epitaxial layers of SiC have been reported to limit the current and voltage ratings in devices and have contributed to degraded performance and failure. [1]

Si Power Device Reliability Benchmarks

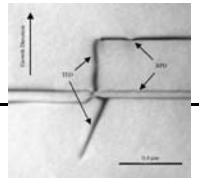
- IGBT Modules are around 10's to a few FIT (10^{-9} failures per device operation hour)
  - Gate drivers now have a higher FIT than IGBT device
  - IGBT Package and device-related failures account for about 35% of the faults in motor drive circuits

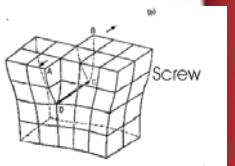
- IGCT operation in rail inverter applications has indicated > 45 years MTBF and an associated 6 FIT

Key Improvement Question

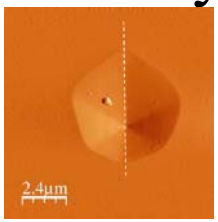
- Can FIT meet or exceed Si parts to take advantage of projected 3-fold increase in power density (SiC) ?
  - This improved power density typically means higher operating temperatures, greater thermal cycling, higher impressed electric fields, etc. - ALL IN OPPOSTION TO IMPROVED RELIABILITY

Defects in WBG Material

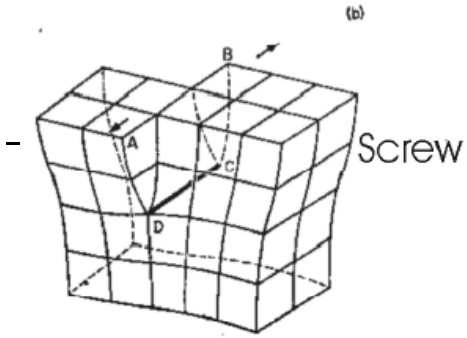




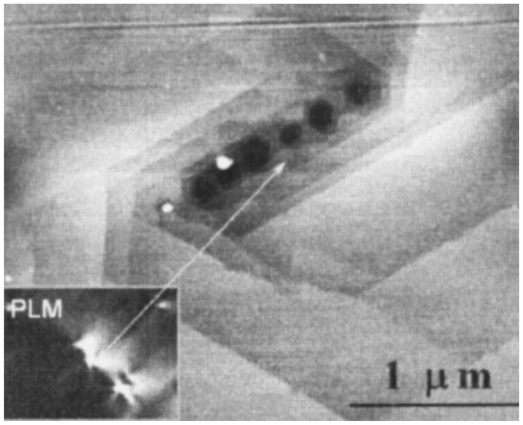
- SiC
  - Micropipes nearly eliminated (< 2.5 per cm^2)
  - Threading Screw Dislocation (TSD) density is around 1000 per cm^2
  - Basal Plane Dislocation (BPD) density is a few to 10's per cm^2
  - Threading Edge Dislocation (TED) density is 100's to 1000's per cm^2
  - Result is a derating of voltage or current density by a factor of 2 or more
- GaN
  - Bulk defect densities can exceed 10^6 per cm^2



Threading Screw Dislocation



Reference [2]



Reference [3]

Substrate screw dislocation propagates into epi-layer depending on the epitaxial growth method.

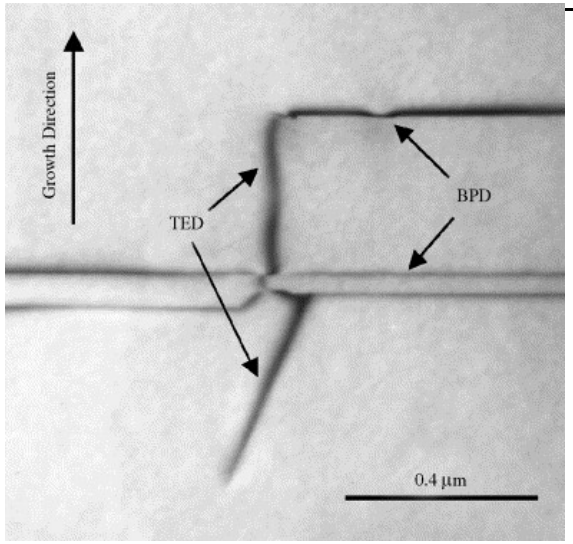
One dislocation will:

- Reduce V_{BD} by 5-35%;
- Soften the breakdown;
- Highly localized current may concentrate in the dislocation resulting in microplasmas.

The defects may also result in reduction of charge carrier lifetime.

Currently, the density is 1000 - 3000 cm^{-2}

Basal plane dislocations (BPDs)



Reference [4]

BPDs are one of the troublesome defects in SiC material.

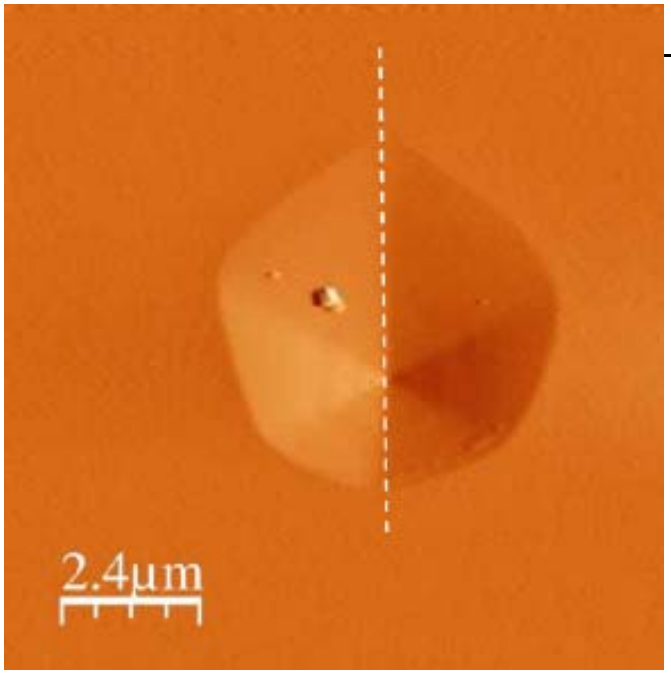
Stacking faults originate from the BPD causing:

- increase in V_F under constant current for **bipolar SiC devices**;
- increase of reverse-biased leakage;
- decrease in forward-biased current in **unipolar devices**.

The main source of BPDs in epitaxial layer is from propagation of BPDs present in the substrate.

Currently, the density is below 10 cm^{-2} due to improvements in bulk and epitaxial growth.

Threading edge dislocations (TEDs)



Reference [5]

Usually one dimensional defects on the wafer surface.

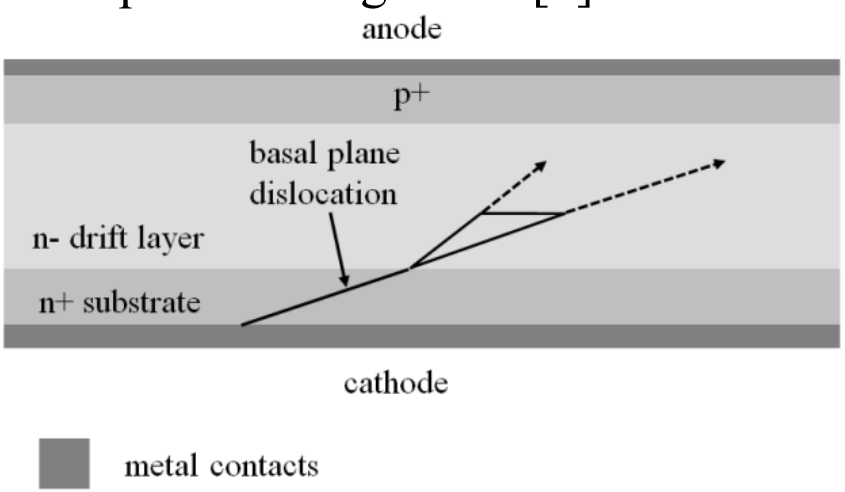
They occur by insertion or removal of an extra half plane of atoms between two lattice atomic planes.

Currently, the density several 10^3 cm^{-2}.

Diodes with higher TEDs densities have **higher leakage current** and slightly **lower breakdown** voltage compare to those without dislocations.

pin Diodes in SiC suffering from basal plane dislocation glide and stacking fault creation during the on-state. [1, 6]

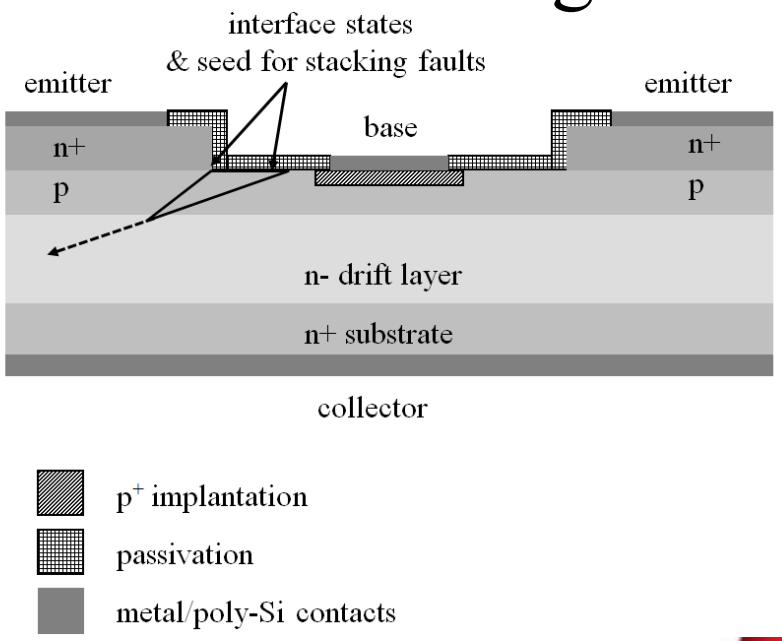
- Over current during on-state causes an increase in the recombination energy being absorbed to create and further extend existing material defects. These increased defects lead to more charge carrier recombination, thus delivering more energy to the crystal and increasing the effective forward voltage drop (increasing the power dissipated in the device).
  - Specifically, Basal Plane Dislocations (BPD) expand into triangular shaped stacking faults [7]



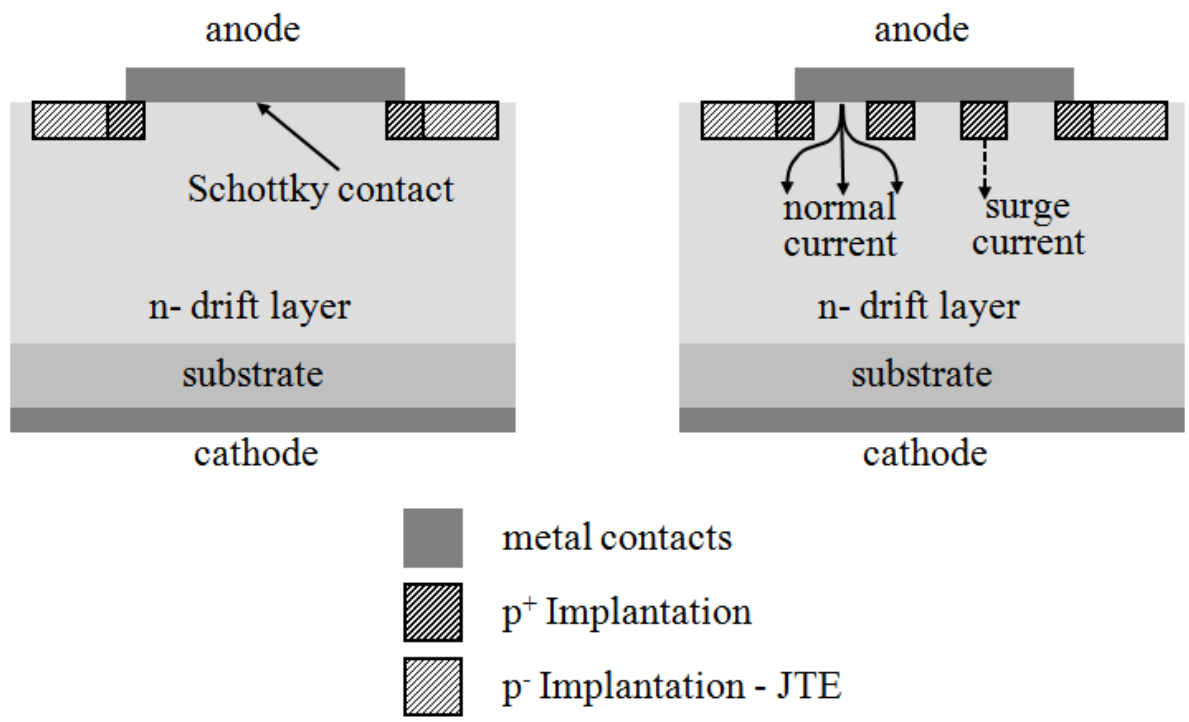
The 4º to 8º off-orientation of crystallographic c-axis for epitaxial layer can cause BPD growth inclined to surface originating from epi-layer and substrate interface with a growing stacking fault.

SiC Power BJT

- Interface states near the emitter act as recombination sites and affect the current gain.
- Stacking faults grow from the surface and degrade the current gain by up to 50% after a few hours of operation.
  - This can be mitigated by proper processing of surface passivation layers [7].



Schottky and Junction Barrier Schottky (JBS) Diodes in SiC

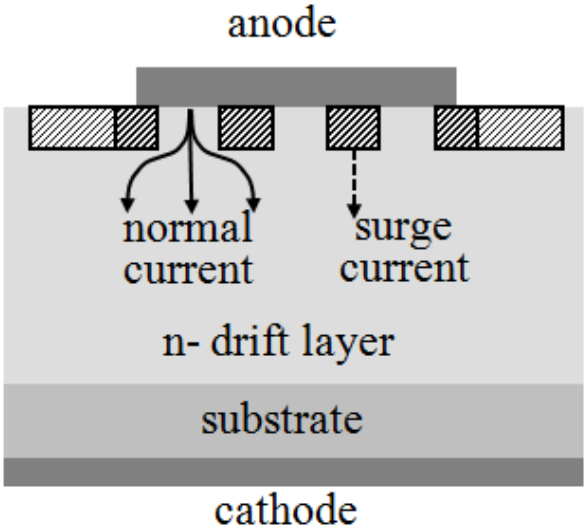


•Failure of Schottky Diodes reported as dv/dt stress causing breakdown due to excess charge generation in space charge region under reverse bias in an area with dislocation defects. [8]

•JBS diode structures have been shown to handle surge current densities at least twice as high as for Schottky diodes. [9,10]

JBS Diodes in SiC – Problem or Not?

However, operation of JBS diodes has shown increased forward voltage over time due to stacking faults increasing charge carrier recombination and impeding charge flow just as in other SiC bipolar devices. [7]

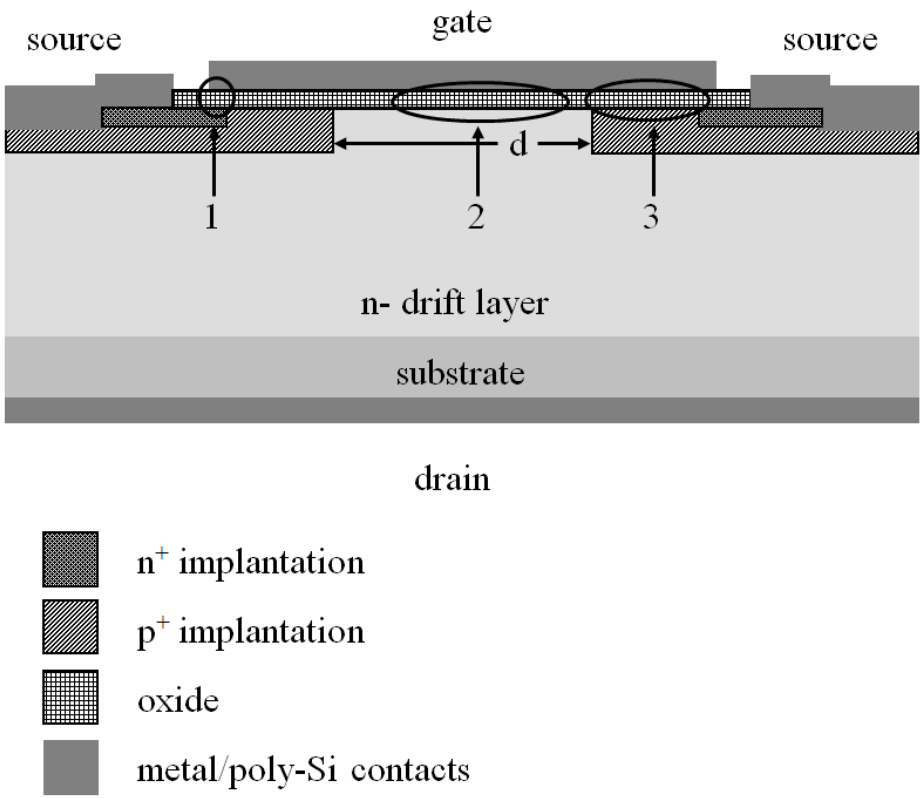


Infineon's 2nd generation Schottky diodes are reported to have a failure rate of less than 0.15 ppm.

However, Cree's SiC JBS diodes have achieved a failure rate of less than 0.5 failures per billion operational hours (0.5 FIT). [11]

SiC MOS-devices

Oxide Growth on SiC



- Annealing at high temperatures after p-body and n^+-source region implants results in the need for oxide growth afterward.
- Oxide grows in an area with high nitrogen doping (area 1).
- Oxide growth over epi-layer is grown with few defects (area 2).
- Oxide grows in an area with high aluminum doping (area 3).

Electric field stress is determined by oxide thickness and gate voltage; choices limited due to targets for threshold voltage and transconductance. Due to permittivity differences between SiO_2 and SiC, the electric field strength in the oxide is typically 3 times higher than in the SiC. Control of the parameter d (pitch in p-body) modifies the field.

SiC - Dielectric Interface State Density

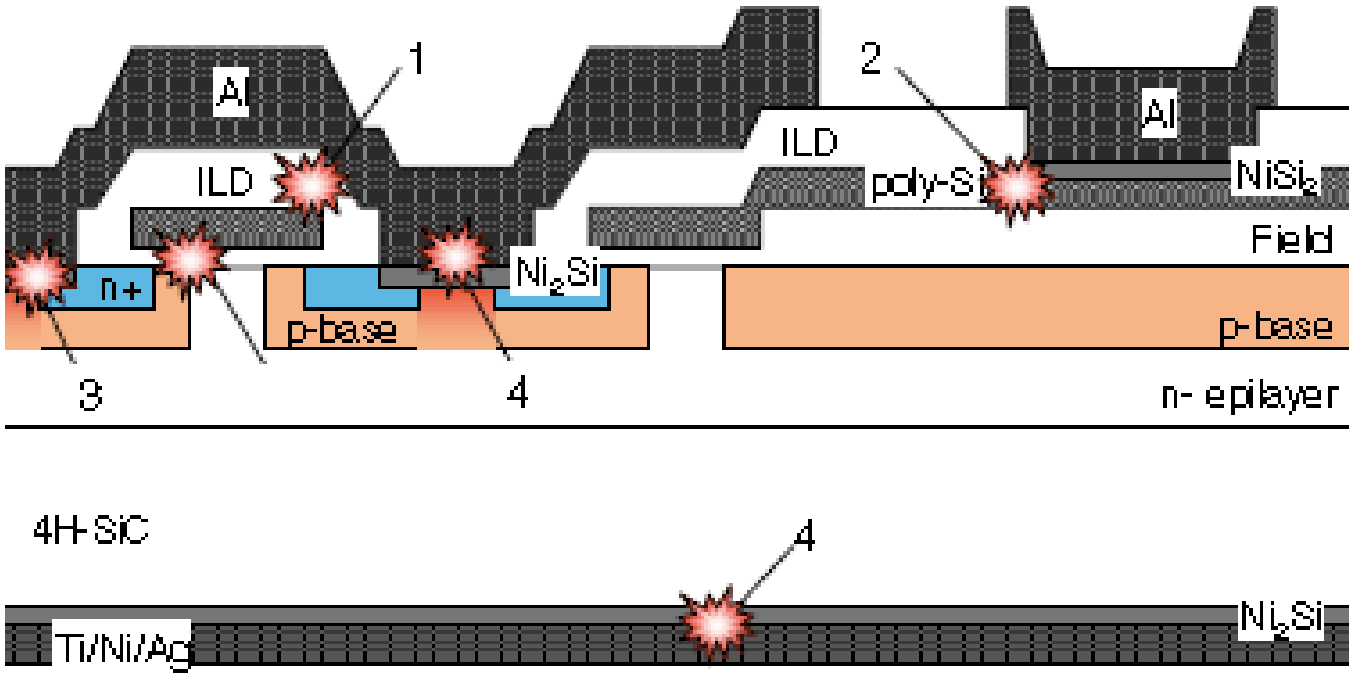
- Various intrinsic defects not related to dopants or impurities are observed at the SiC/SiO_2 interface.
- SiC has a higher surface density of atoms per unit area compare to Si, resulting in a higher density of dangling Si- and C-bonds and carbon cluster at the interface.
- Defects located in the near-interfacial oxide layer may appear in the energy gap of SiC and act as traps for electrons.
- Low channel mobility in 4H-SiC is directly linked to very high interface state densities in the SiO_2/SiC interface.
- Interface state densities reduction plays a critical role in increasing of channel mobility and improving the high temperature performance, as well as the reliability of power SiC MOSFETs.

Dielectric Improvements

- Reduction of the interface state density and improve the device reliability by nitric oxide post-oxidation annealing.
  - This reduces carbon clusters at the interface thus increasing the channel mobility and the dielectric quality.
  - One promising solution is carefully formed an oxide-nitride-oxide (ONO) dielectric on 4H-SiC [7, 12]

•Cree has shown with Time Dependent Dielectric Breakdown (TDDB) measurements that the breakdown field in the oxide is 10 MV/cm and a corresponding MTTF over 10^9 years. [13]
•Cree has demonstrated threshold voltage shifts of about 1 V under High Temperature Gate Bias (HTGB) tests.

Problems with Al for Operation above 200 ºC [12]



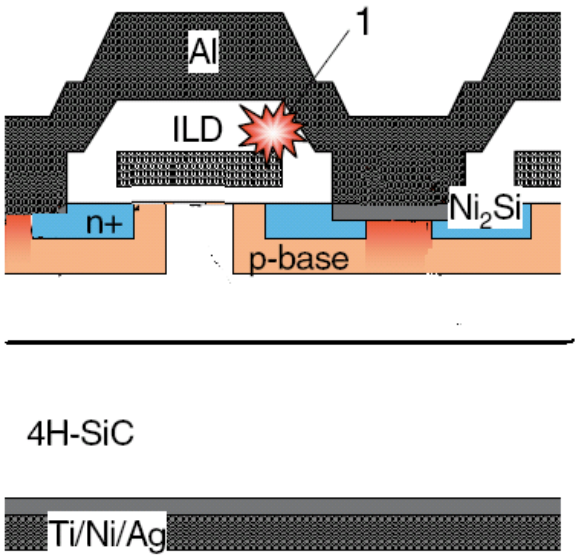
1. Interlayer dielectric erosion
2. Al spearing to poly-Si gate
3. Ni_2Si contact disappearance
4. Electrode delamination

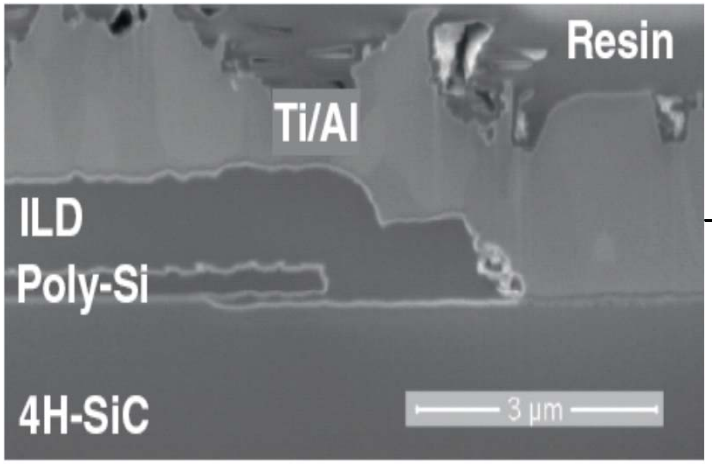
Interlayer dielectric erosion (IDE)

Al electrodes erode and penetrate the underlying interlayer dielectric and finally reach the poly-Si gate, resulting in the gate-source short-circuit.

Failure occurs within only 2 hours of storage time at 500 ^{o}C.

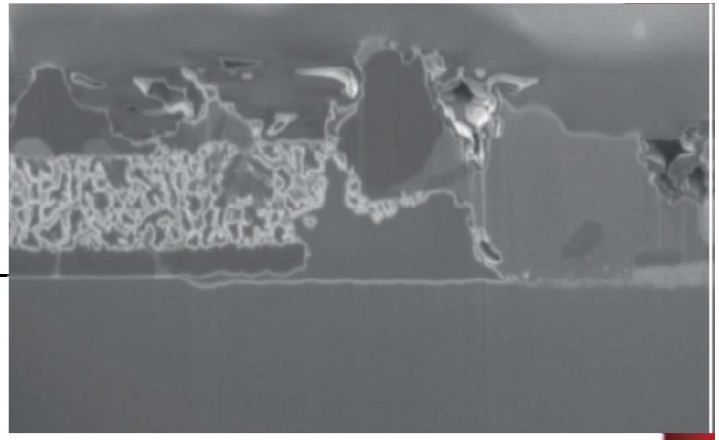
The erosion progression depends on the temperature and the quality of the silicate glass.

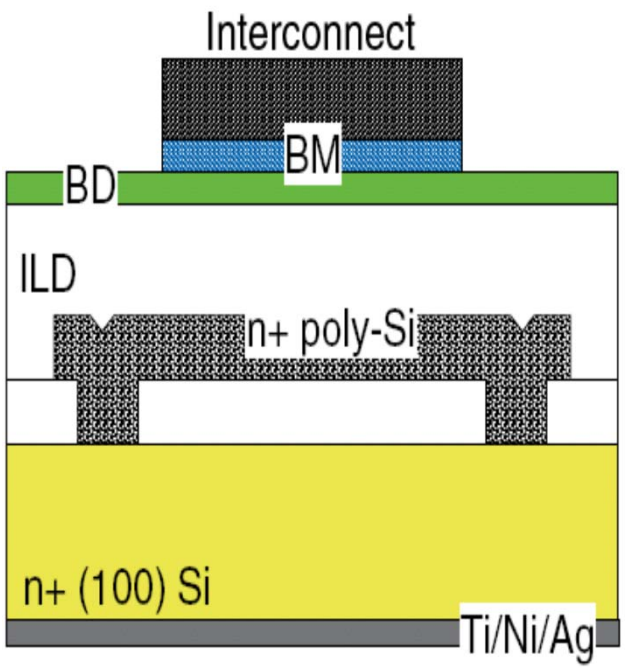




Before

After





To prevent IDE:

-Use Si (1 wt%) - doped Al which effectively reduces the dissolution and movement;

- Use of a barrier metal (BM) preventing the movement of Al into the underlying material (50 nm of Ta and 150 nm of TaN;

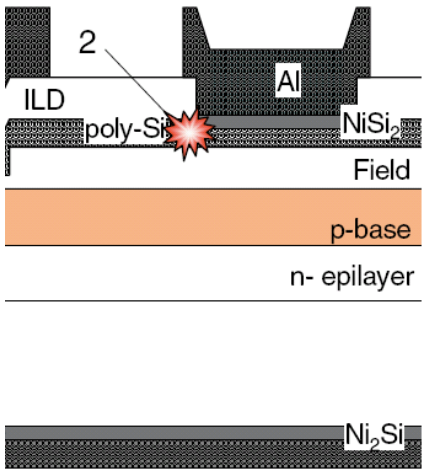
- Deposition of a barrier dielectric (BD) over the silicate glass interlayer dielectric.

Al spearing in poly-Si

Al spears (or spikes) are seen in the gate located between the Al-interconnect and the gate after 2 hours of storage at 500 ^{o}C.

Caused by massive movement of Al of the gate interconnect into the poly-Si gate.

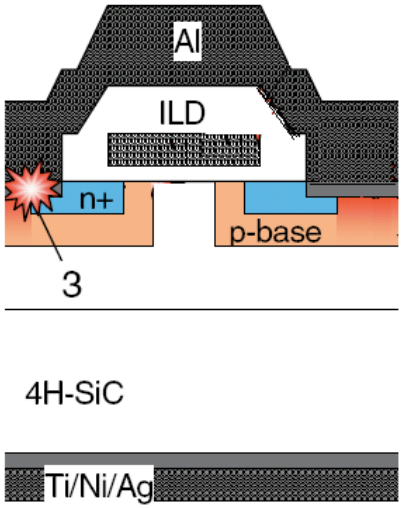
Al spears extend to the channel region along the poly-Si gate and reduce the gate oxide, causing a dielectric breakdown failure and finally a gate-to-source short circuit.



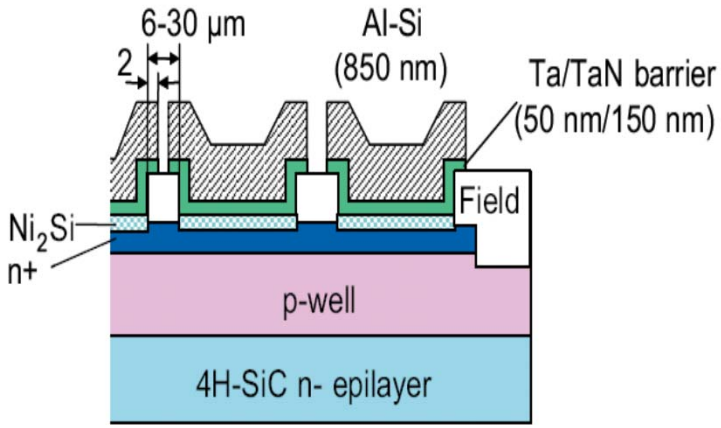
Ni_2Si contact degradation

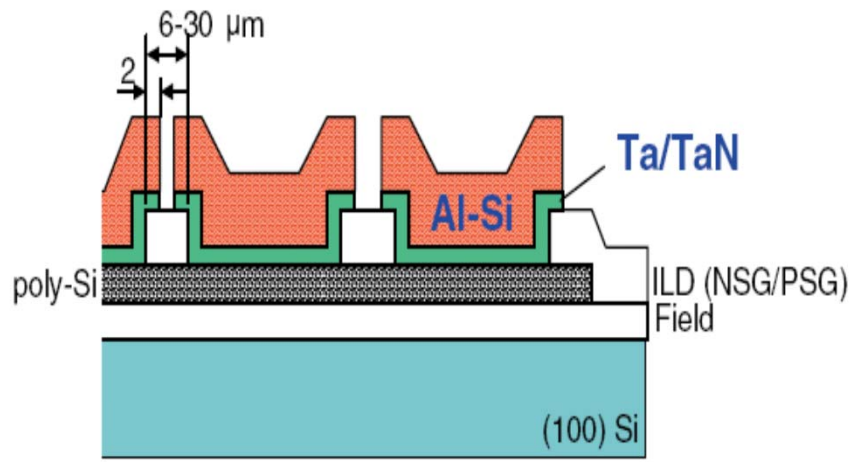
Ni_2Si-based ohmic contacts degrade in connection with the Al interconnect, such as the contacts on the n+ source region.

Contact disconnection is observed after 32 hours at 500 ^oC. Al starts to react with Ni_2Si, decomposing it and forming $NiAl_3$ and Si.



Mitigation of Al spearing and Ni_2Si contact disappearance





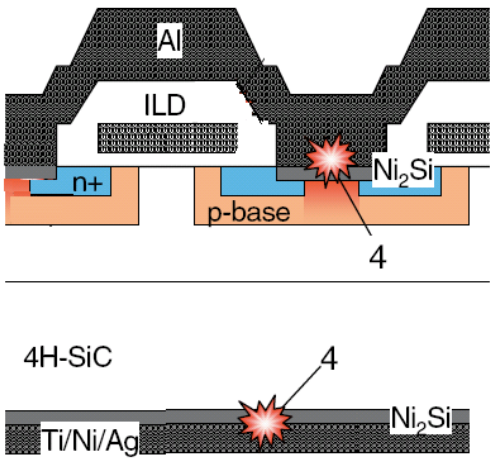
To prevent the Al spikes in poly-Si gate a combination of 1 wt% Si-doped Al interconnect and Ta/TaN barrier metal can be used.

Electrode delamination

Ni_2Si contacts have low resistance and are used as ohmic contacts on n-type 4H-SiC.
A common technique for fabricating Ni_2Si contacts is to deposit a thin Ni film followed by rapid-thermal annealing at 950 -1050 ^oC.

Surface segregation of carbon due to the annealing causes the upper metallization layer to delaminate.

To avoid: remove surface segregated carbon before the metallization process. However, delamination can still occur probably due to movement of carbon back to the surface over time. Further processing with H_2 sintering followed by O_2 treatment.



SiC JFET

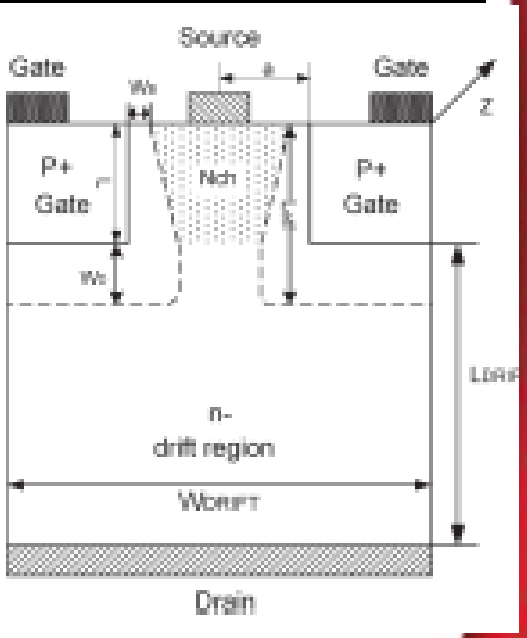
3.5 kV - **Vertical JFET** R_{on} = 30 mΩ-cm^2 **[19]**;

4 kV- **Vertical JFET** R_{on} = 45 mΩ-cm^2 **[20]**;

5.3 kV **Static Expansion Channel JFET-Normally-off**
R_{on} = 69 mΩ-cm^2 **[21]**;

11.1 kV - **Normally-off TI-VJFET** R_{on} = 124 mΩ-cm^2 **[22]**;;

4.5 kV - **Cascode based on SiC VJFET** R_{on} = 1.2 Ω **[23]**.



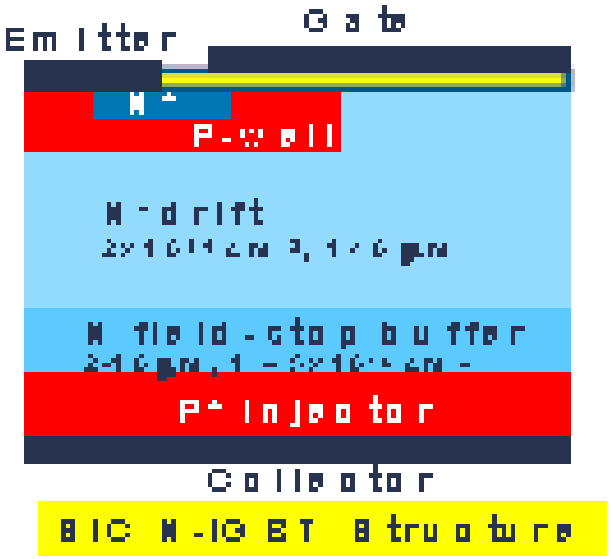
SiC IGBT

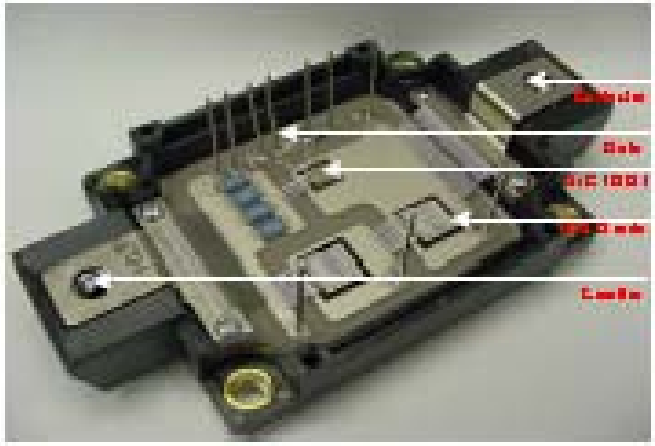
10-kV ***P*-IGBT** on SiC was reported in 2005 **[24]**;

12 kV ***P*- IGBT** R_{on} = 14 mΩ-cm^2 **[25]**;

13 kV ***N*- IGBT** R_{on} = 22 mΩ-cm^2 **[26]**;

12 kV, 10 A **N-IGBT [34]**





SiC Thyristors

First SiC symmetrical thyristors 700 V, at 6 A V_F = 3.9 V **[27]**;

1.77 kV, at 100 A and 200 °C V_F = 4 V **[28]**;

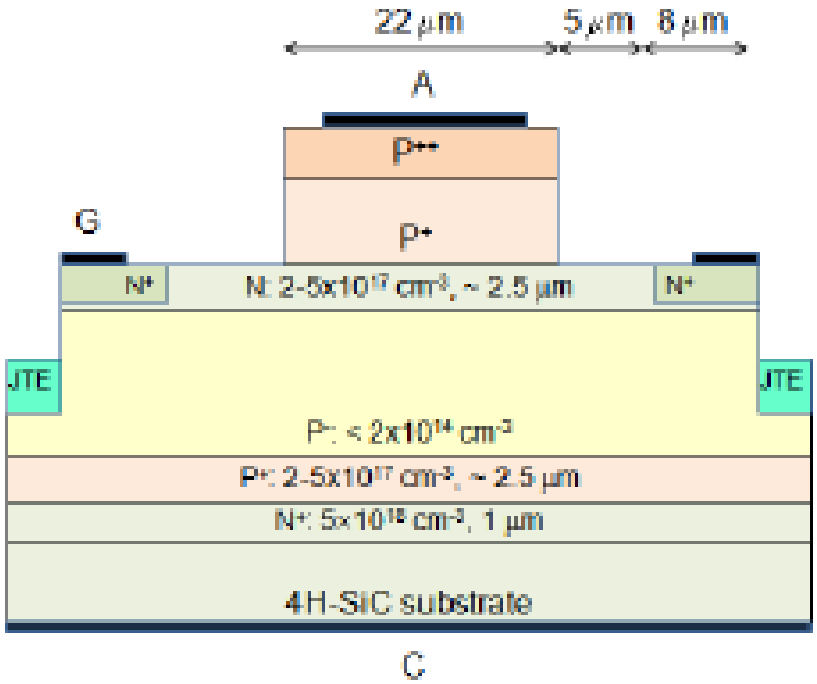
2.6 and 3.1 kV at 12 A V_F = 6.5 V **[29]**;

7 kV at 300 A/cm^2 and 25 °C V_F = 3.66 V;
at 300 A/cm^2 and 224 °C V_F = 3.1 V, **[30]**;

4.5-kV *P*-type GTO 4.6 V at 25 A/cm^2 turn-off energy loss 9.88 mJ **[31]**;

7.8 kV Graded etched junction termination extension thyristors V_F = 3.9 V at 100 A/cm2 R_{on} = 5.3 mΩ-cm^2 **[32]**;

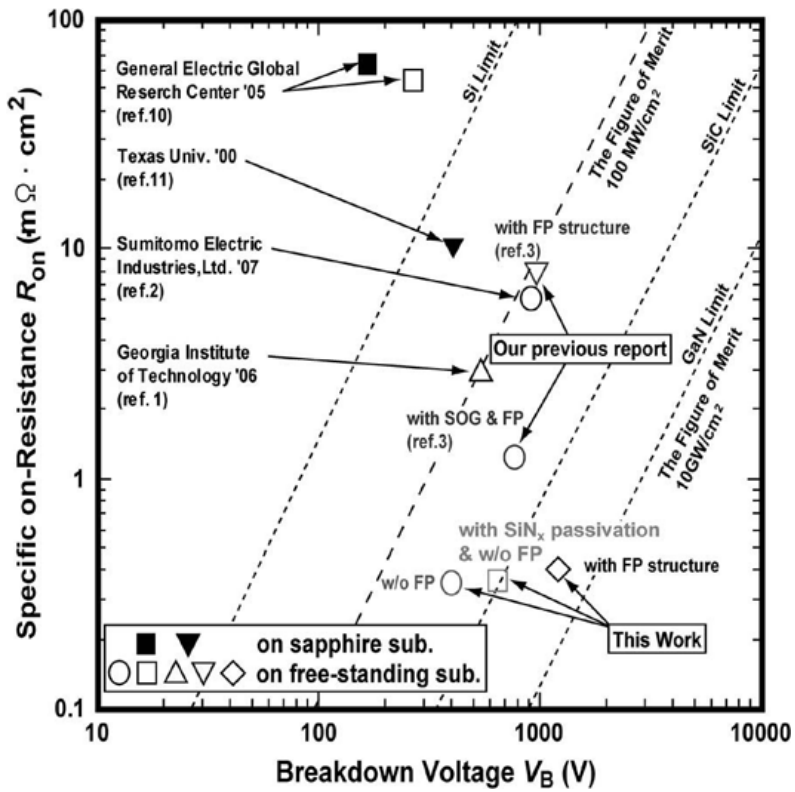
12.7 kV SiC commutated GTO V_F = 6.6 V, leakage current less than 1 x 10^{-3} A/cm^2 at 9 kV and at 250 °C, at 100 A/cm^2 **[33]**;

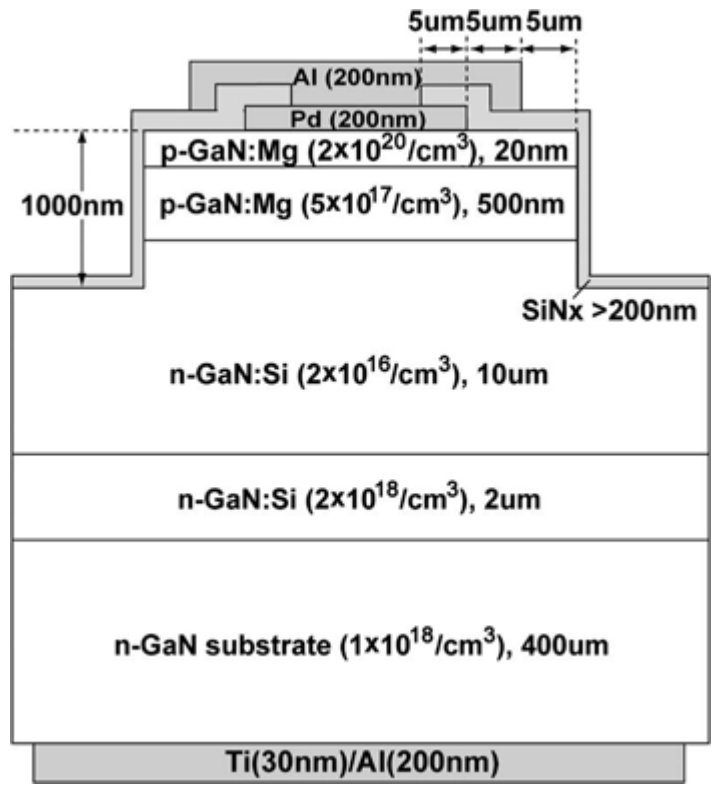


GaN

GaN Diodes

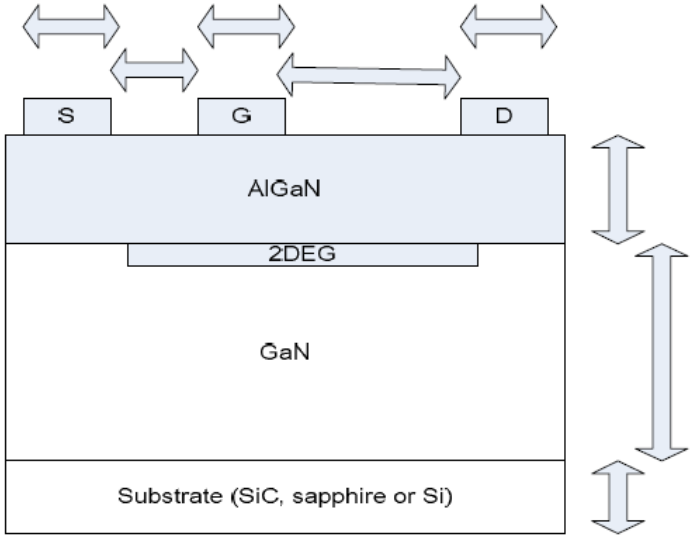
- GaN *pn*-junction diode with silicon nitride (SiNx) passivation and aluminum field-plate (FP) structure (1.1 kV breakdown). [14]



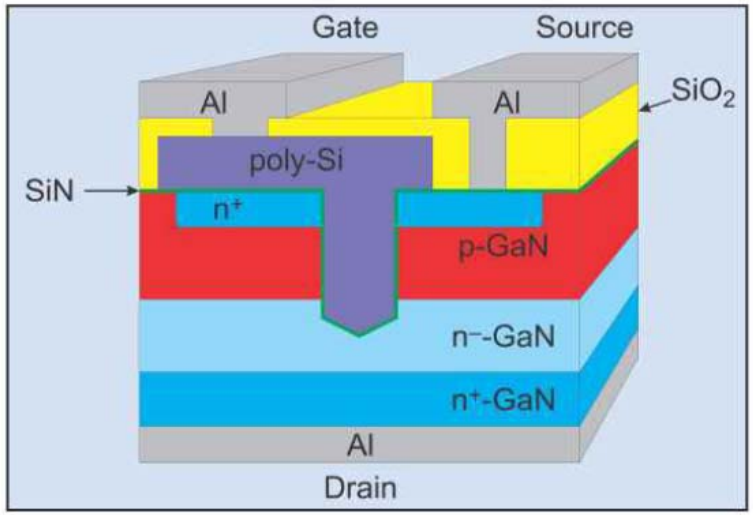


GaN Transistors

- Lateral HEMT (HFET or MODFET)
  - Channel formed at AlGaN/GaN interface.
  - Due to bandgap differences, 2D electron gas formed which promotes high conductivity electron flow.



- Vertical Structures
  - Lateral or Vertical Gate Designs

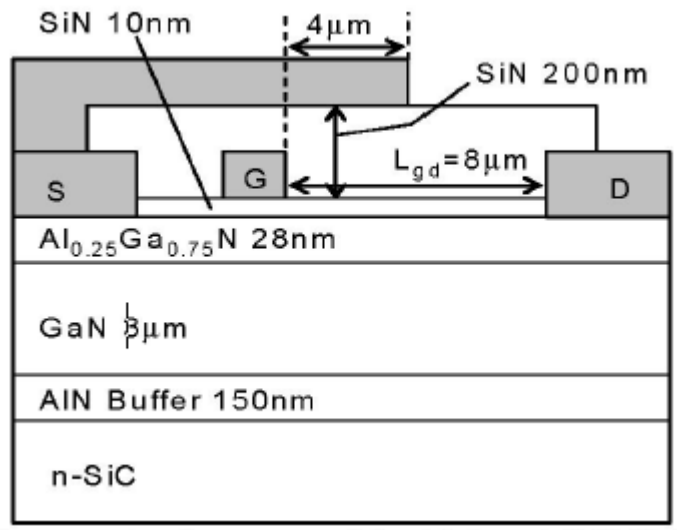


GaN Transistors – Some Issues

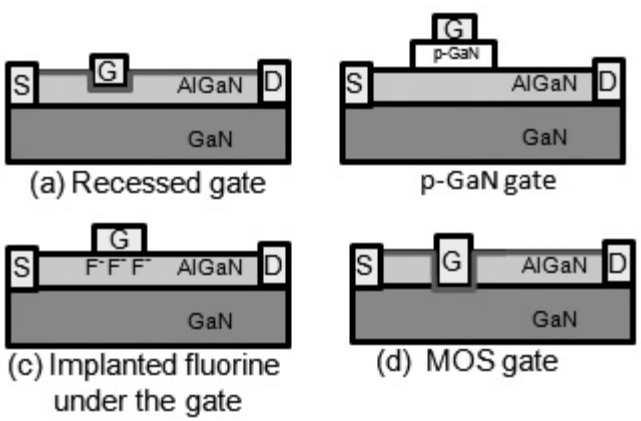
- Need normally-off devices.
- Lattice mismatch between AlN buffer layer, GaN, and substrate material (Si, SiC, or sapphire) introduces defects.
  - GaN substrates becoming available
- Current degradation (collapse) due to electron trap sites from surface defects and dislocations.
  - SiN passivation has been used to help mitigate. [15]
- Lateral structures are field limited. Incorporating field plates improves breakdown capability.

Trends in Lateral Devices

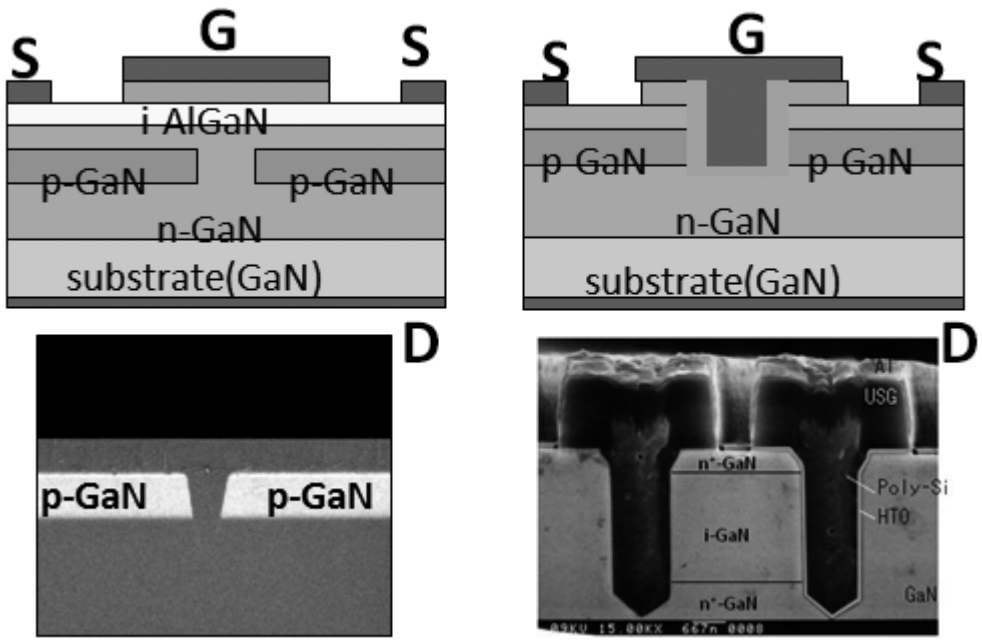
- GaN HEMT with field plate and Metal-Insulator-Semiconductor (MIS) gate. [15]
  - Reduces electric field at gate edge



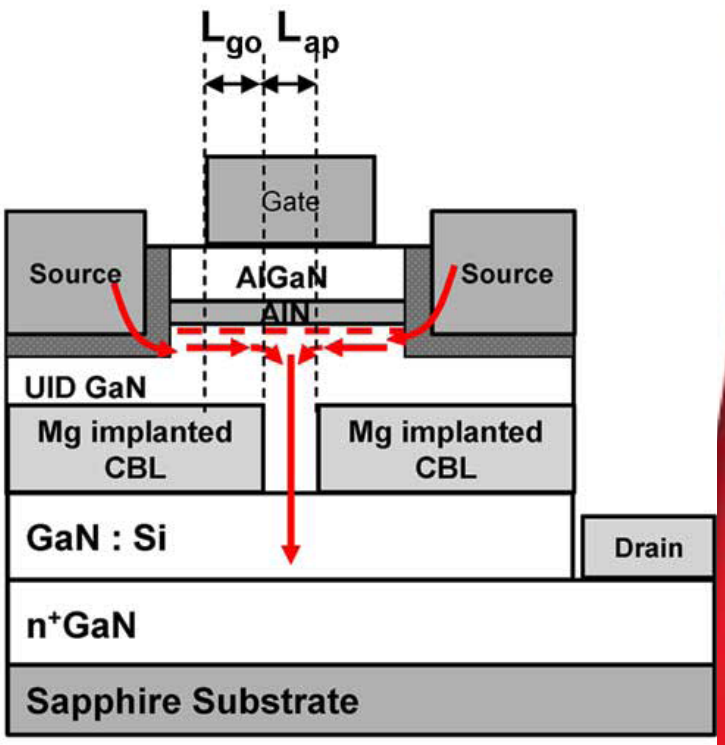
- Proposed normally-off structures [16]



Vertical Transistors



Lateral and Vertical Gate structures. [17]

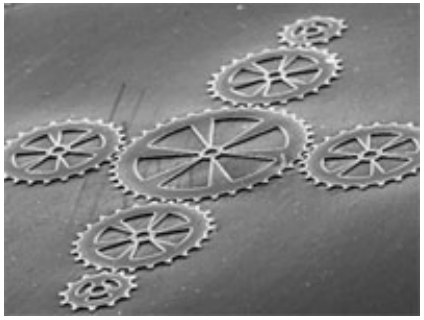


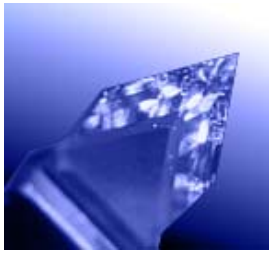
Current Aperture Vertical Electron Transistor (CAVET) with Mg doped current blocking layer reaching 5000 A/cm^2. [18]

Carbon (Diamond)

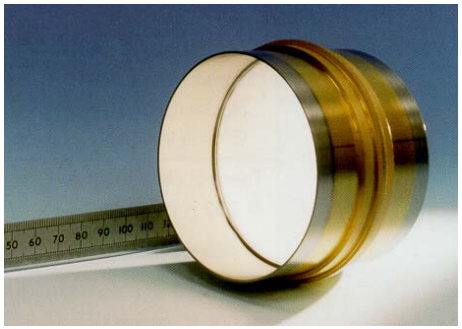
Diamond applications

Mechanical

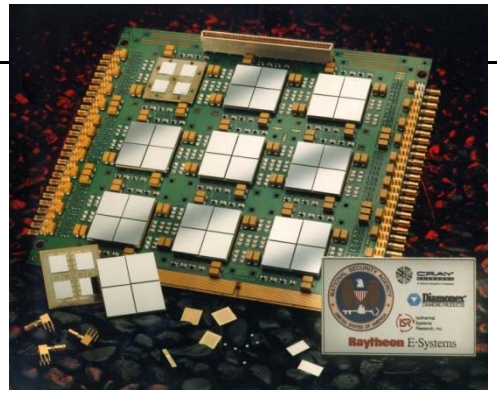


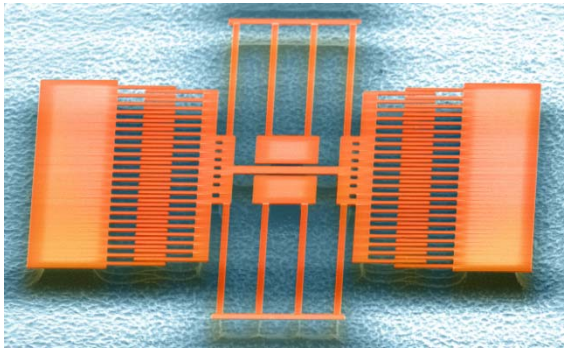


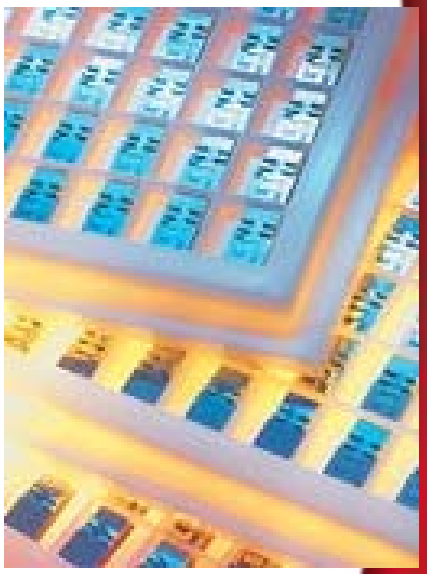
Optical



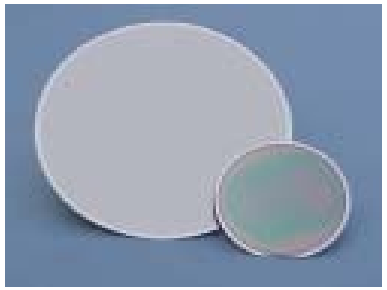
Thermal

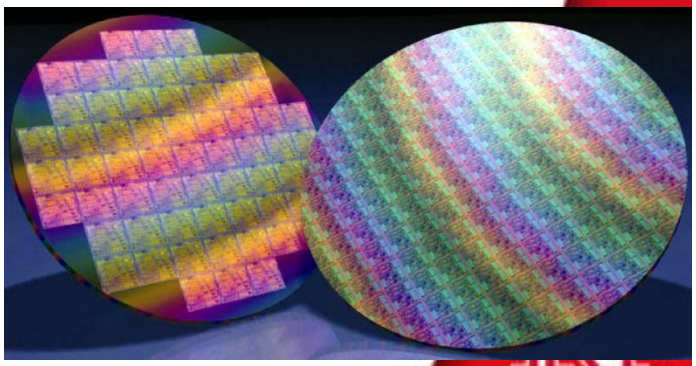




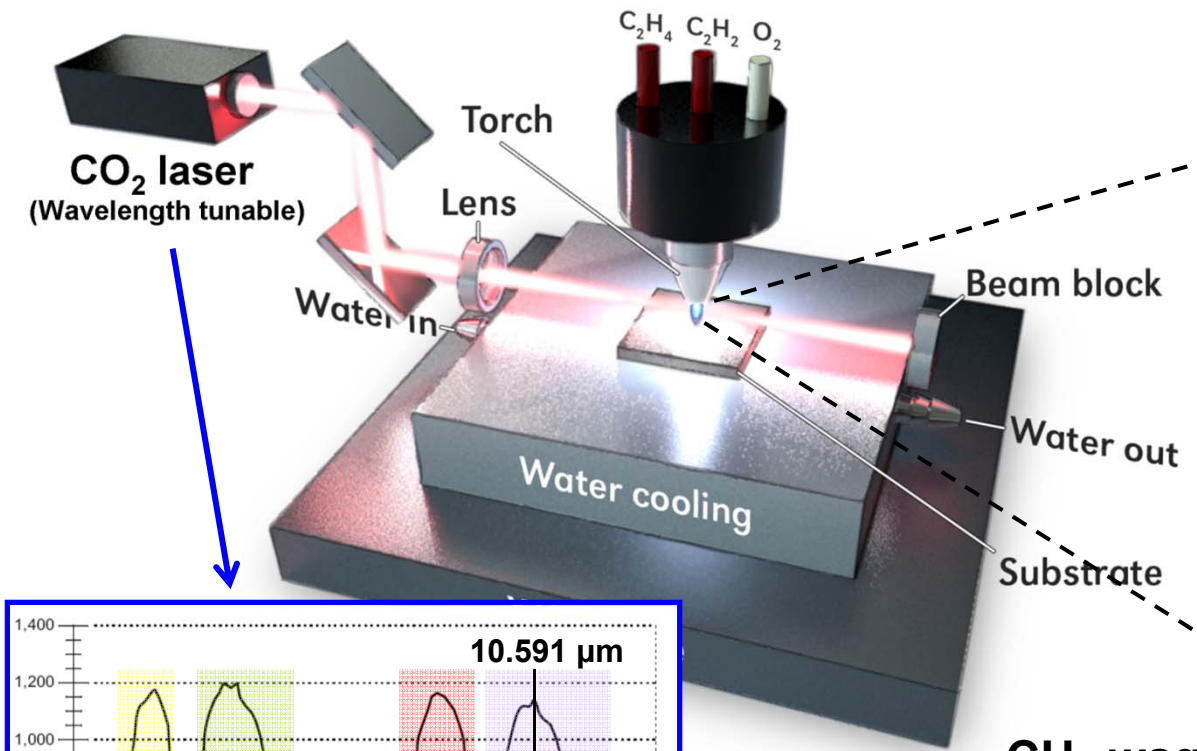


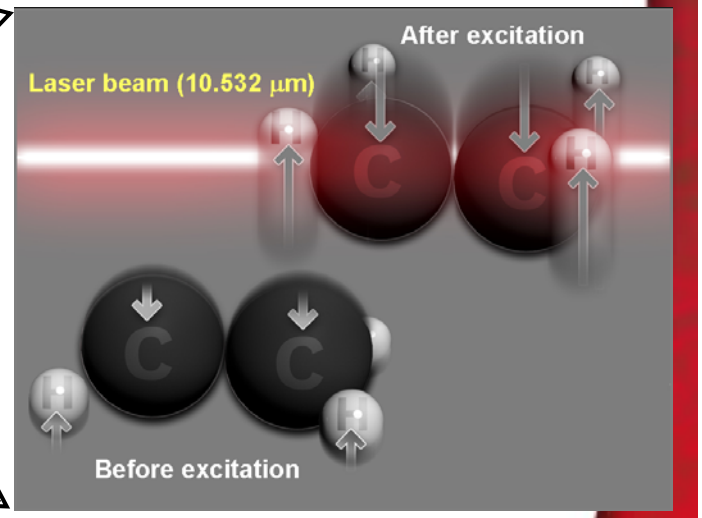
Electrical

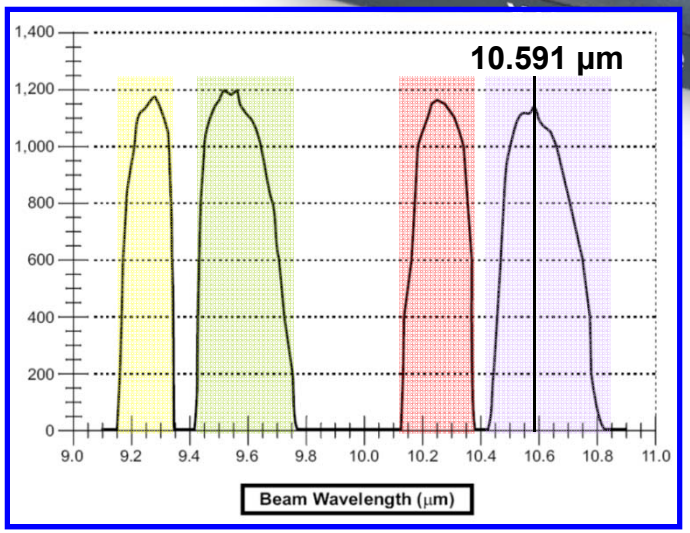




Approach: Laser-induced multi-energy processing





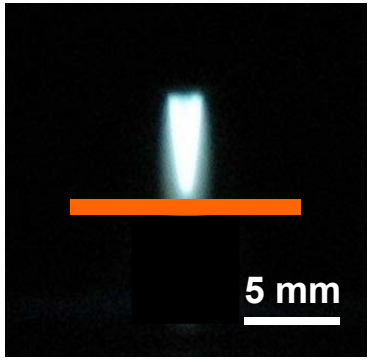


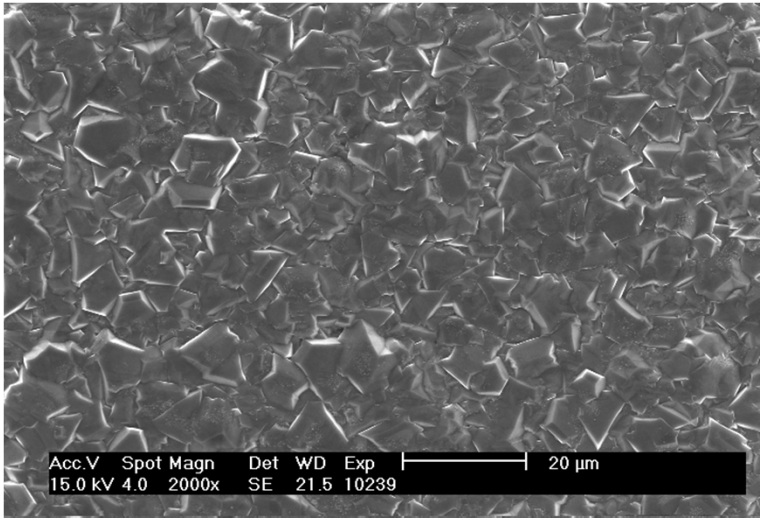
CH_2-wagging mode: *10.534 μm*

CO_2 laser: *10.532 μm*

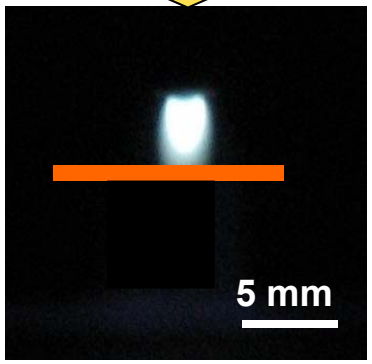
Enhancement of diamond film crystal growth

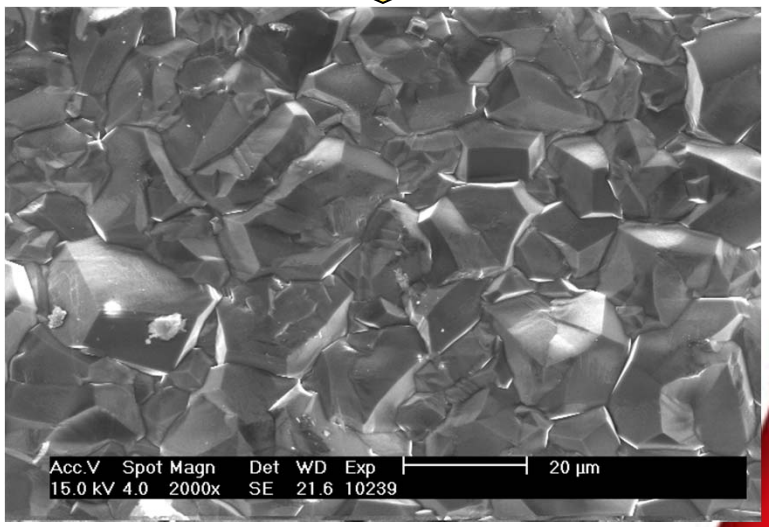
No laser irradiation



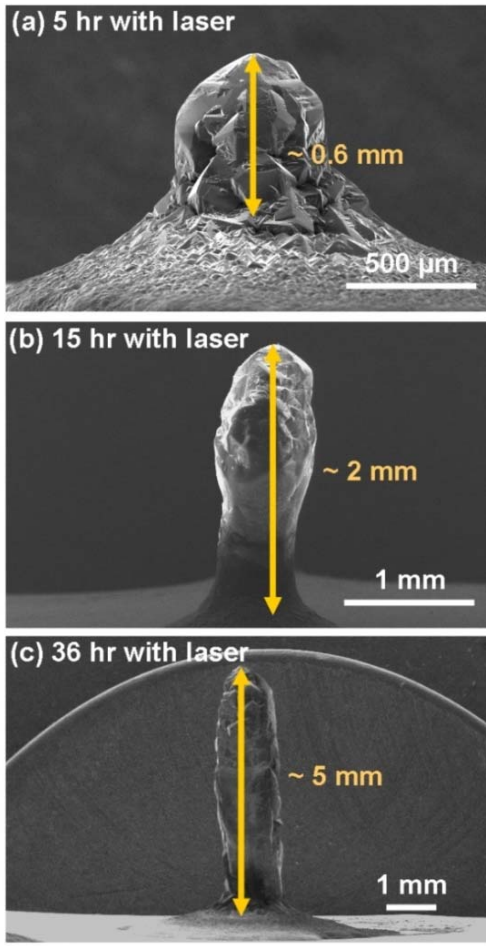


Irradiated by tuned CO_2 laser (10.532 µm, 800 W)

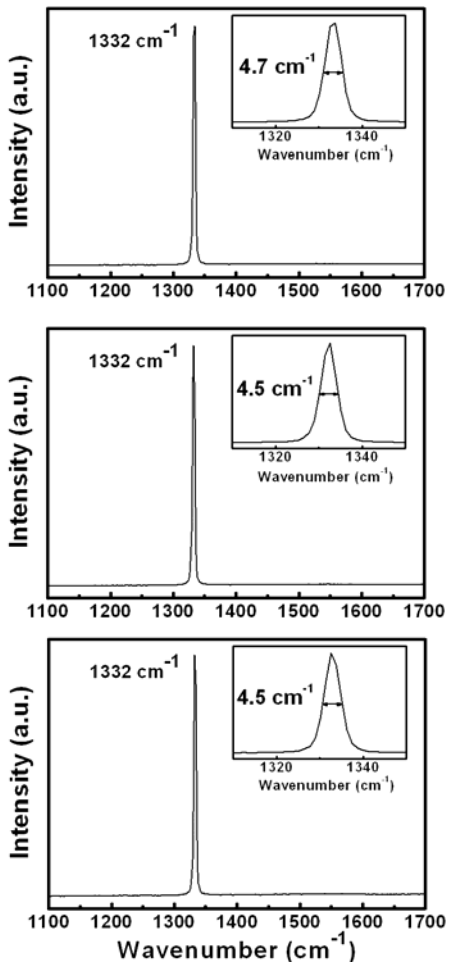




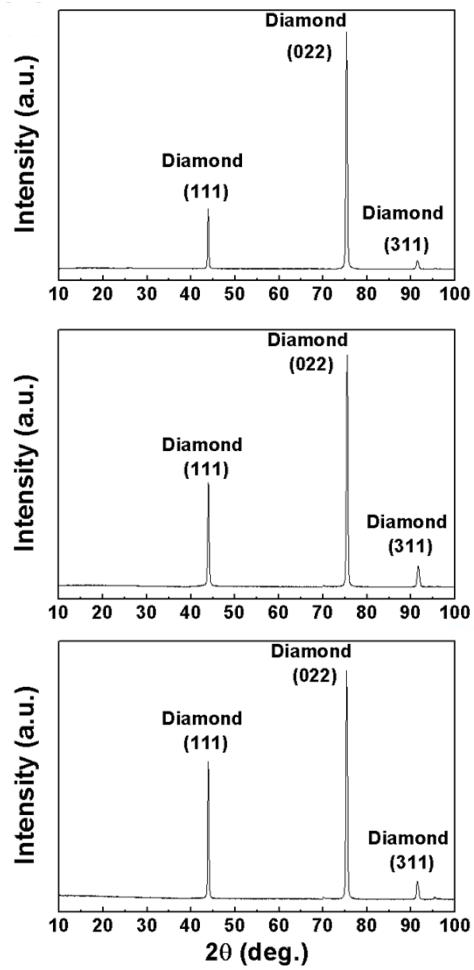
SEM



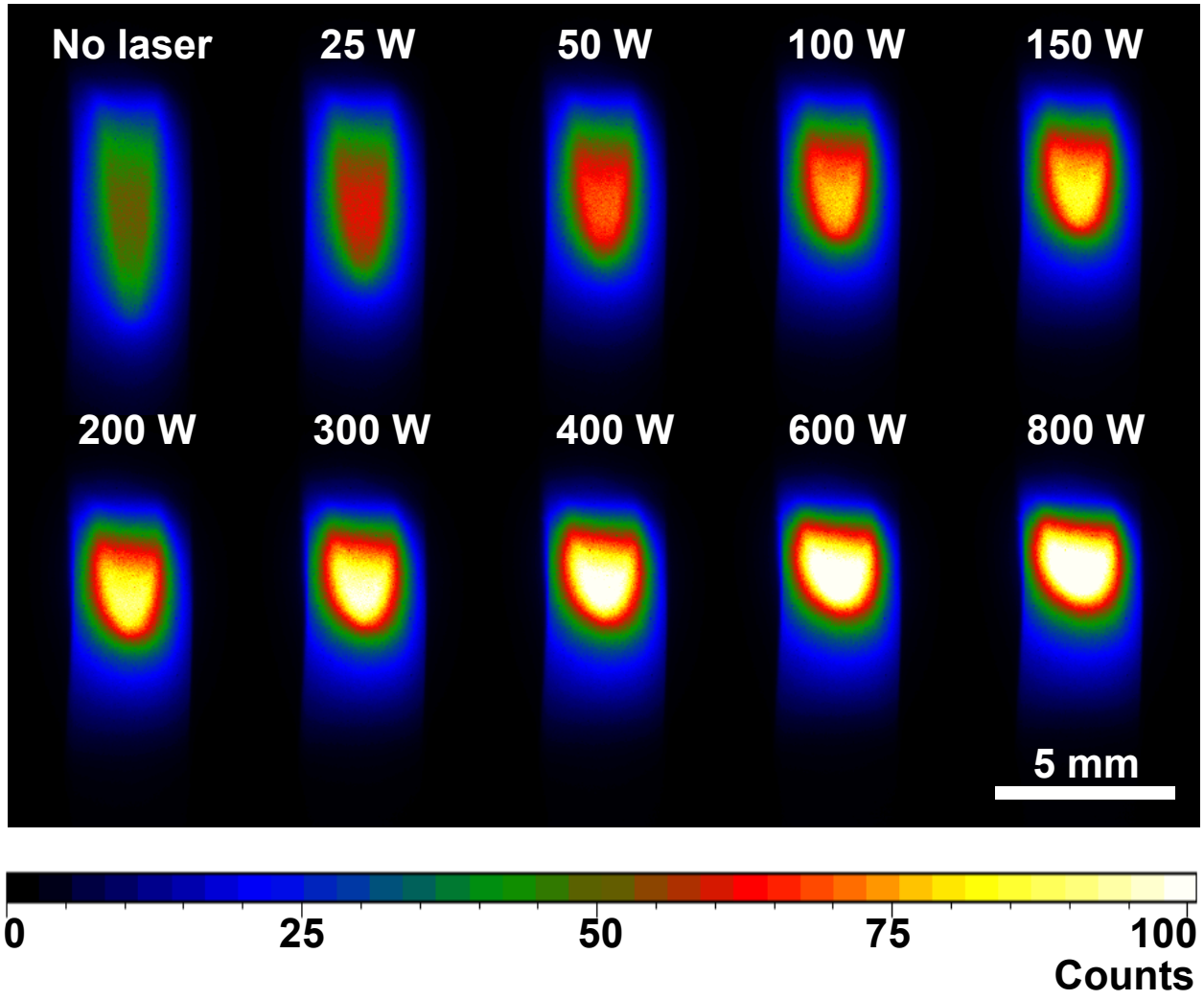
Raman



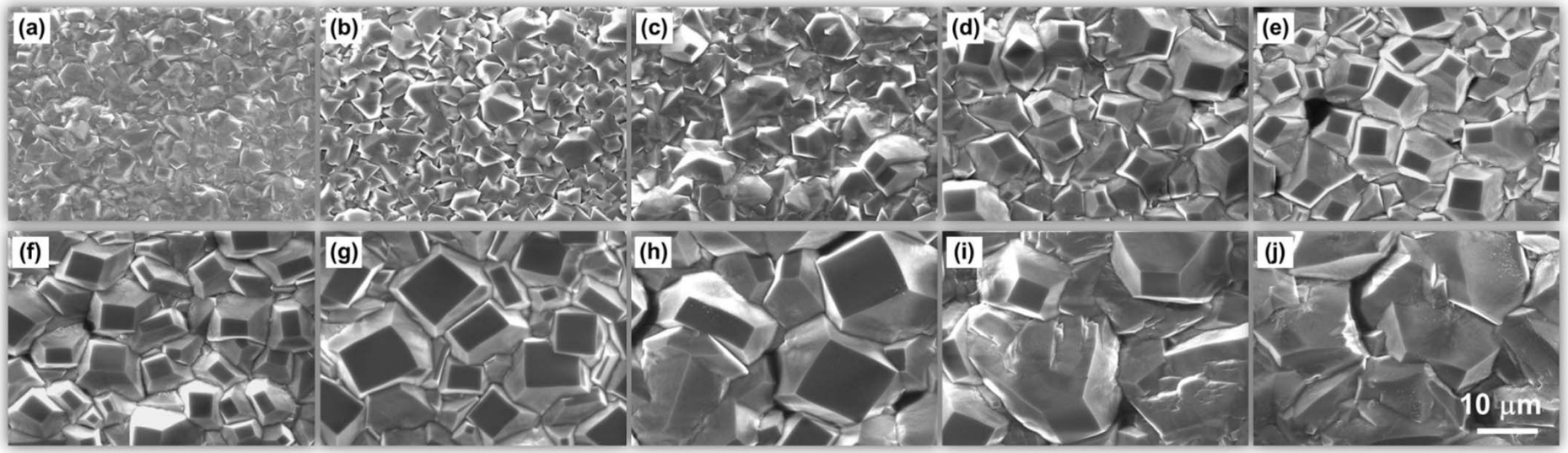
XRD



Excitation at different laser powers

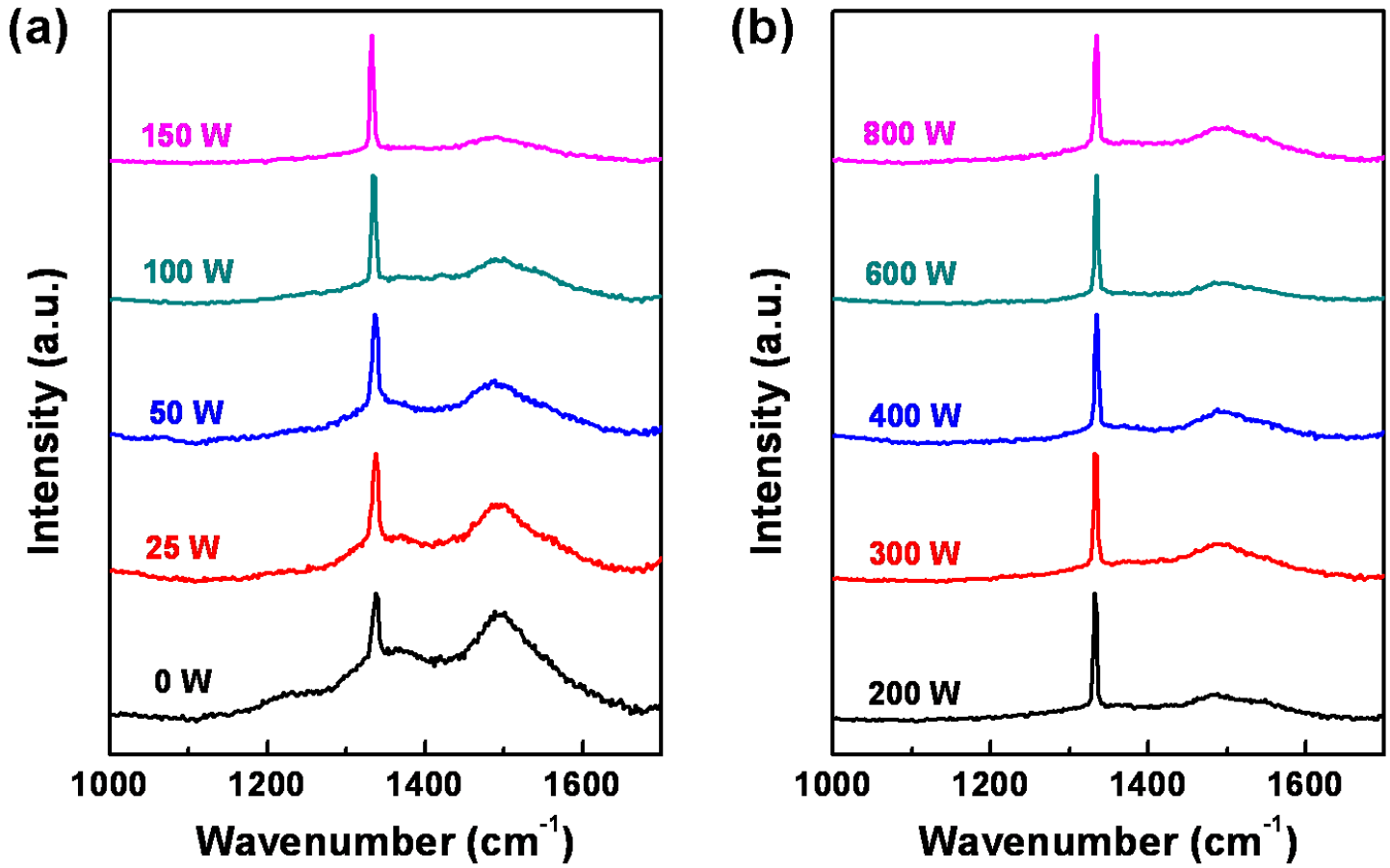


Deposition of diamond films



SEM images of diamond films deposited for 1 hour with laser excitation at (a) 0, (b) 25 , (c) 50 , (d) 100, (e) 150 , (f) 200, (g) 300, (h) 400, (i) 600, and (j) 800 W.

Raman spectra



References

[1] "High-Power Switching in Semiconductors – What is Beyond Silicon Thyristor?" K. Shenai, P. G. Neudeck, M. Dudley, and R. F. Davis, *Energytech*, pp. 1-6, 2011.

[2] "Structural Defects in SiC. Georgios Manolis," Jean Carlos da Conceicao Lorenzzi, based on the lecture of Prof. John Stoemenos.

[3] "Superscrew dislocations in silicon carbide: Dissociation, aggregation, and formation," Xianyun Ma, *J. Appl. Phys.* 99, 063513, 2006.

[4] "Propagation behavior of threading dislocations during physical vapor transport growth of silicon carbide (SiC) single crystals," Noboru Ohtani, Masakazu Katsuno, Hiroshi Tsuge, Tatsuo Fujimoto, Masashi Nakabayashi, Hirokatsu Yashiro, Mitsuru Sawamura, Takashi Aigo, Taizo Hoshino, *Journal of Crystal Growth*, Vol 286, pp. 55–60 , 2006.

[5] "Effect of threading screw and edge dislocations on transport properties of 4H–SiC homoepitaxial layers," S. I. Maximenko, J. A. Freitas, Jr., R. L. Myers-Ward, K.-K. Lew, B. L. VanMil, C. R. Eddy, Jr., D. K. Gaskill, P. G. Muzykov and T. S. Sudarshan, *J. Appl. Phys.* 108, 013708, 2010.

[6] "Development of 10 kV 4H-SiC power DMOSFETs," S.H. Ryu, S. Krishnaswami, A. Agarwal, J. Richmond, and J. Palmour, *Mater. Sci. Forum*, pp. 457–460, 2004.

[7] "Reliability of SiC Power Devices and its Influence on their Commercializing – Review, Status, and Remaining Issues," Michael Treu, Roland Rupp, and Gerald Sölkner, *Reliability Physics Symposium (IRPS)*, pp. 156-161, 2010.

[8] "On the dv/dt Rating of SiC Schottky Power Rectifiers," K. Acharya and K. Shenai, *Proc. Power Electronics Technology Conference*, pp. 672-677, 2002.

[9] "A surge for current stable and avalanche rugged SiC merged pn Schottky diode blocking 600V especially suited for PFC applications," M. Treu, R. Rupp, C. S. Tai, P. Blaschitz, J. Hilsenbeck, H. Brunner, D. Peters, R. Elpelt, and T. Reinmann, *Mat. Scie. For.*, Vols. 600-602, pp. 935-603, 2007.

[10] "Surge current ruggedness of silicon carbide Schottky and merged-pin-Schottchy diodes," B. Heinze, J. Lutz, M. Nuemeister, R. Rupp, and M. Holz, *Proc. 20th Int. Symp. Power Sem. Dev. IC's*, pp. 245-248, 2008.

[11] "Commercially Available Cree Silicon Carbide Power Devices: Historical Success of JBS Diodes and Future Power Switch Prospects," Mrinal K. Das, *CS MANTECH Conference*, 2011.

[12] "Reliability issues of SiC power MOSFETs toward high junction temperature operation," Satoshi Tanimoto, and Hiromichi Ohashi, *Phys. Status Solidi* A 206, No. 10, pp. 2417–2430 , 2009.

[13] "SiC MOSFET Reliability Update," Mrinal K. Das, Sarah Haney, Jim Richmond, Anthony Olmedo, Jon Zhang, and Zoltan Ring, *Materials Science Forum*, Vols. 717-720, pp. 1073-1076, 2012.

References (2)

[14] "Over 3.0 GW/cm^2 Figure-of-Merit GaN p-n Junction Diodes on Free-Standing GaN Substrates," Yoshitomo Hatakeyama, Kazuki Nomoto, Naoki Kaneda, Toshihiro Kawano, Tomoyoshi Mishima, and Tohru Nakamura, *IEEE Electron Device Letters*, Vol. 32, No. 12, 2011.

[15] "On the Suitability of Gallium-Nitride (GaN) Based Automotive Power Electronics," S. Dargahi and Sheldon S. Williamson, *Vehicle Power and Propulsion Conference (VPPC)*, pp. 1-6, 2010.

[16] "GaN Power Device and Reliability for Automotive Applications," Tetsu Kachi, Daigo Kikuta, Tsutomu Uesugi, *Reliability Physics Symposium (IRPS)*, pp. 3D.1.1-3D.1.4, 2012.

[17] "Automotive Applications of GaN Power Devices," Tetsu Kachi, Masakazu Kanechika, and Tsutomu Ugesugi, *Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1-3, 2011.

[18] "Enhancement and Depletion Mode AlGaN/GaN CAVET With Mg-Ion-Implanted GaN as Current Blocking Layer," Srabanti Chowdhury, Brian L. Swenson, and Umesh K. Mishra, *Electron Device Letters*, Vol. 29, No. 6, pp. 543-545, 2008.

[19] "The vertical silicon carbide JFET - a fast and low loss solid state power switching device," P. Friedrichs, H. Mitlehner, R. Schorner, K. O. Dohnke, R. Elpelt, and D. Stephani. *Graz, Austria : s.n., 2001*, EPE 2001.

[20] "Stacked high voltage switch based on Sic VJFETs," P. Friedrichs, H. Mitlehner, R. Schorner, K.O. Dohnke, R. Elpelt and D. Stephani. Cambridge, UK : s.n., *ISPSD*, pp. 139-142, 2003.

[21] "5kV 4H-SiC SEJFET with Low RonS of 69m12cm2," K. Asano, Y. Sugawara, T. Hayashi, S. Ryu, R. Singh, J. Palmour, and D. Takayama. Santa Fe : s.n., *ISPSD'02*, pp. 61-64, 2002.

[22] "Normally-off 4H-SiC trench-gate MOSFETs with high mobility," J. Wua, J. Hua, J. H. Zhao, X. Wang, X. Li, L. Fursin, T. Burke, *Solid-State Electronics*, Vol. 52, No. 6, pp. 909-913, 2008.

[23] "High voltage, modular switch based on Sic VJFETs - first results for a fast 4,5kV/1.2 Ohm configuration," P. Friedrichs, H. Mitlehner, R. Schorner, K. O. Dohnke, R. Elpelt, and D. Stephani, Linkiiping : s.n., *ECSCRM*, 2002 .

[24] "10 kV trench gate IGBTs on 4H-SiC," Q. Zhang, H.R. Chang, M. Gomez, C. Bui, E. Hanna, J. A. Higgins, T. I. Smith, and J. R. Williams, *The 17th International Symposium on Power Semiconductor Devices and Ics*, pp. 303–306, 2005.

[25] "12 kV 4H-SiC p-IGBTs with record low specific on-resistance," Q. Zhang, C. Jonas, J. Sumakeris, A. Agarwal, and J. Palmour. Otsu, Japan : s.n., *Int. Conf. Silicon Carbide and Related Materials (ICSCRM)*, 2007.

[26] "A 13 kV 4H-SiC N-channel IGBT with lowRdiff,on and fast switching," M. Das, Q. Zhang, R. Callanan, C. Capell, J. Claytou, M. Donfrio, S. Haney, F. Husna, C. Jonas, J. Richmond, and J. J. Sumakeris. Otsu, Japan : s.n., *Int. Conf. Silicon Carbide and Related Materials (ICSCRM)*, 2007.

References (3)

[27] "700-V Asymmetrical 4H-SiC Gate Turn-Off Thyristors (GTOs)," A. K. Agarwal, J. B. Casady, L. B. Rowland, S. Seshadri, R. R. Siergiej, W. F. Valek, and C. D. Brandt, *IEEE Electron Device Letters*, Vol. 18, p. 518, 1997.

[28] "The First Demonstration of the 1 cm x 1 cm SiC Thyristor Chip-," A. K. Agarwal, B. Damsky, J. Richmond, S. Krishnaswami, C. Capell, S. H. Ryu, and J. W. Palmour, Santa Barbara : s.n., *The 17 International Symposium on Power Semiconductor Devices & IC's*, pp. 195 – 198, 2005.

[29] "2600 V, 12 A, 4H-SiC, asymmetricalgate turn-off (GTO) thyristor development," A. K. Agarwal, S. H. Ryu, R. Singh, O. Kordina, and J. W. Palmourl, *Materials Science Forum*, Vols. 338 - 342, pp. 1387-1390, 2000.

[30] "7 kV 4H-SiC GTO Thyristors," S. V. Campen, A. Ezis, J. Zingaro, G. Storaska, R. C. Clarke, V. Temple, M. Thompson, and T. Hansen, *MRS Proceedings*, Vol. K7.7, pp.742, 2002.

[31]"Design and Characterization of High-Voltage Silicon Carbide Emitter Turn-off Thyristor," J. Wang, and A. Q. Huang, *IEEE Transactions on Power Electronics*, Vol. 24, No. 5, pp.1189-1197, 2009.

[32] "High-Voltage 4H-SiC Thyristors With a Graded Etched Junction Termination Extension," G. Paques, S. Scharnholz, N. Dheilly, D. Planson, R. W. De Doncker, *Electron Device Letters*, Vol. 32, No. 10, pp.1421-1423, 2011.

[33] "12.7 kV Ultra High Voltage SiC Commutated Gate Turn-off Thyrsitor: SICGT," Y. Sugawara, D. Takayama, K. Asano, A. Agarwal, S. Ryu, J. Palmour, S. Ogata, *Power Semiconductor Devices and ICs, Proceedings. ISPSD '04, The 16th International Symposium*, pp. 289-292, 2004.

[34] "*Comparison study of 12kV n-type SiC IGBT with 10kV SiC MOSFET and 6.5kV Si IGBT based on 3L-NPC VSC applications,*" S. Madhusoodhanan, K. Hatua, S. Bhattacharya , S. Leslie, S. Ryu, M. Das, A. Agarwal, and D. Grider, *Proc. IEEE ECCE*, pp. 310-317, 2012, Raleigh, NC.

Other Bibliographic Sources

1. "Recent developments of high power converters for industry and traction applications," S. Bernet, *IEEE Trans. Power Electron*, Vol. 15, No. 6, pp. 1102-1117, 2000.
2. "12-19kV 4H-SiC p–i–n diodes with low power loss," Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, *Osaka, Japan : s.n., 2001. 13th Int. Symp. Power Semiconductor Devices and Ics*, pp. 27–30, 2001.
3. "Large Area, Ultra-high Voltage 4H-SiC p-i-n Rectifiers," R. Singh, K. G. Irvine, D. C. Capell, J. T. Richmond, D. Berning, and A. R. Hefner, IEEE Trans. Electron. devices, Vol. 49, No. 12, pp. 2308-2316, 2002.
4. "4H-SiC power bipolar junction transistor with a very low specific on-resistance of 2.9 mΩ • cm2," J. Zhang, P. Alexandrov, T. Burke, and J. H. Zhao, *IEEE Electron Device Lett*., Vol. 27, No. 5, pp. 368–370, 2006.
5. "1800 V NPN bipolar junction transistors in 4H-SiC," S. Ryu, A. K. Agarwal, R. Singh, and J. W. Palmour, *IEEE Electron Device Lett*., Vol. 22, pp. 124–126, 2001.
6. "4H-SiC NPN bipolar junction transistors with BVCEO > 3200 V," C. Huang, and J. A. Cooper, Jr. *The 14th International Symposium on Power Semiconductor Devices and Ics*, pp. 57–60, 2002.
7. "A high voltage (1,750V) and high current gain (β= 24.8) 4H-SiC bipolar junction transistor using a thin (12 μm) drift layer." J. H. Zhao, J. Zhang1, P. Alexandrov, X. Li, and T. Burke, Materials Science Forum, Vols. 457-460, pp. 1173-1176, 2004.
8. "Implantation-free 4H-SiC bipolar junction transistors with double base epilayers," J. Zhang, and T. Burke, *IEEE Electron Device Lett.*, Vol. 29, No. 5, pp. 471–473, 2008.
9. "A high current gain 4H-SiC NPN power bipolar junction transistor," J. Zhang, Y. Luo, P.Alexandrov, L.Fursin, and J. H. Zhao, *IEEE Electron Device Lett*., Vol. 24, pp. 327–329, 2003.
10. "High voltage (>1 kV) and high current gain (32) 4H-SiC power BJTs using Al-free ohmic contact to the base," Y. Luo, J. Zhang, P. Alexandrov, L. Fursin, J. H. Zhao, and T. Burke, *IEEE Electron Device Lett*., Vol. 24, No. 11, pp. 695–697, 2003.
11. "High-current-gain SiC BJTs with regrown extrinsic base and etched JTE," H. Lee, M. Domeij, R. Ghandi, C.M. Zetterling, and M. Östling, *IEEE Transaction on Electron Devices*, Vol. 55, No. 8, pp. 1894-1898, 2008.
12. "High temperature characterization of 4H-SiC bipolar junction transistors," S. Krishnaswami, A. Agarwal, J. Richmond, C. Capell, S.-H. Ryu, J. Palmour, B. Geil, D. Katsis, and C. Scozzie, *Materials Science Forum*, Vol. 527–529, pp. 1437–1440, 2006.
13. "High Power(500V-70A) and High Gain(44-47) 4H-SiC Bipolar Junction Transistors," J.Zhang, P.Alexandrov, and J. H. Zhao, *Materials Science Forum*, Vols. 457-460, pp. 1149-1152, 2004.
14. "Recent progress in SiC single crystal wafer technology," N. Ohtani, Kona, Hawaii, USA : s.n.*," The 5th International Symposium on Advanced Science and Technology of Silicon Materials (JSPS Si Symposium)*, 2008.

15. “1200-V 5.2-mΩ • cm2 4H-SiC BJTs with a high common-emitter current gain,” H. S. Lee, and M. Östling, *IEEE Electron Device Lett.*, Vol. 28, No. 11, pp. 1007–1009, 2007.
16. “6 kV 4H-SiC BJTs with specific on-resistance below the unipolar limit using a selectively grown base contact process,” S. Balachandran, C. Li, P. A. Losee, I. B. Bhat, and T. P. Chow, Jeju Island : s.n., *The 19th International Symposium on Power Semiconductor Devices and Ics*, pp. 293–296, 2007.
17. “4H–SiC BJTs with current gain of 110,” Q. J. Zhang, A. Agarwal, A. Burk, B. Geil, and C. Scozzie, *Solid-State Electronics*, Vol. 52, pp. 1008–1010, 2008.
18. “High-voltage double implanted power MOSFETs in 6H-SiC,” J. N. Shenoy, J. A. Cooper, and M. R. Melloch, *Electron Device Lett*., Vol. 18, No. 3, pp. 93–95, 1997.
19. “4H-SiC RF power MOSFET,” A. Alok, E. Arnold, R. Egloff, J.Barone, J. Murphy, R. Conrad, and J. Burke, *Electron Device Letters*, Vol. 22, No. 12, pp.557- 8, 2001.
20. “950V, 8.7mohm-cm2 high speed 4H-SiC power DMOSFETs,” S. Ryu, C. Jonas, B. Heath, J. Richmond, A. Agarwal and J. Palmour. San Francisco : s.n., *Material Research Society Spring Meeting*, pp. 391-400, 2006.
21. “A self-aligned process for high voltage, short-channel vertical DMOSFETs in 4H-SiC,” M. Matin, A. Saha, and J. A. Cooper, Jr., *IEEE Trans. Electron Devices*, Vol. 51, No. 10, pp. 1721–1725, 2004.
22. “A 1-kV 4H-SiC power DMOSFET optimized for low on-resistance,” A. Saha and J. A. Cooper, *IEEE Trans. Electron Devices*, Vol. 54, No. 10, pp. 2786–2791, 2007.
23. “1.1kV 4H-SiC power UMOSFET’s,” A. K. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt, *IEEE Electron Device Letters*, Vol. 18, No.12, pp.586–588, 1997.
24. “Realization of low on-resistance 4H-SiC power MOSFETs by using retrograde profile in P-body,” K. Fujihira, N. Miura, T. Watanabe, Y. Nakao, N. Yutani, K. Ohtsuka, M. Imaizumi, T. Takami, and T. Oomori, *Materials Science Forum*, Vols. 556-557, pp. 827-830, 2007.
25. “1.4 kV 4H-SiC UMOSFET with low specific on-resistance,” Y. Sugawara, and L. Asano, Kyoto : s.n., *10th International Symposium on Power Semiconductor Devices and ICs*, pp. 119-22, 1998.
26. “27 mΩ-cm2, 1.6 kV power DiMOSFETs in 4H-SiC,” S. H. Ryu, A. Agarwal, J. Richmond, J. Palmour, N. Saks, and J. Williams, Santa Fe : s.n., *14th International Symposium on Power Semiconductor Devices and ICs*, pp. 65-68, 2002.
27. “Development of 8 mΩ−cm2, 1.8 kV 4H-SiC DMOSFETs,” S. H. Ryu, S. Krishnaswami, B. Hull, B. Heath, M. Das, J. Richmond, A. Agarwal, J. Palmour, and J. Scofield, *Mater. Sci. Forum*, Vols. 527–529, No. 2, pp. 1261–1264, 2006.

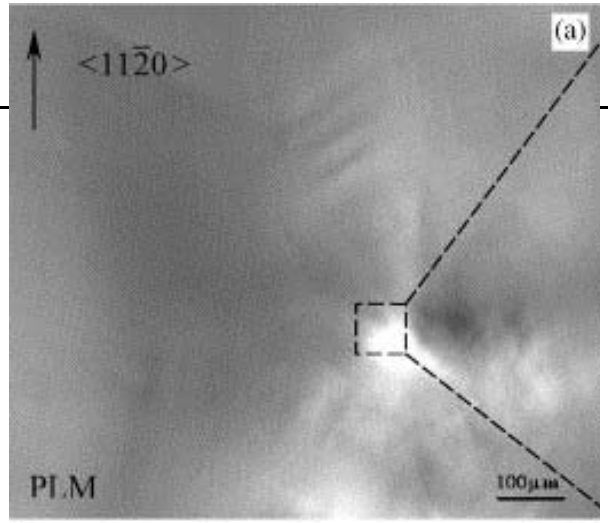
28. “10.3 mohm-cm2, 2 kV power DMOSFETs in 4H-SiC,” S. H. Ryu, S. Krishnaswami, M. Das, B. Hull, J. Richmond, B. Heath, A. Agarwal, J. Palmour, and J. Richmond, *17th Int. Symp. Power Semicond. Devices & IC’s*, pp. 275–278, 2005.
29. *“2.6 kV 4H-Sic lateral DMOSFET’s,”* J. Spitz, M. R. Melloch, J. A. Cooper, Jr., and M. A. Capano, *IEEE Electron Device Letters*, Vol. 19, No. 4, pp. 100-102, 1988.
30. “High-Voltage (3 kV) UMOSFETs in 4H-SiC,” Y. Li, J. A. Cooper, and M. A. Capano, *IEEE Transaction on Electron Devices*, Vol. 49, No. 6, pp. 972-5, 2002.
31. “A 10-kV Large-Area 4H-SiC Power DMOSFET With Stable Subthreshold Behavior Independent of Temperature,” H. Robert, S.Buchoff, S.Van Campen, T.McNutt, A.Ezis, B.Bettina, C.Kirby, M. Sherwin, R.Clarke, and R. Singh, *IEEE Transactions on Electron Devices*, Vol. 55, No. 8, pp. 1807-1815, 2008.
32. “10 kV 123 mΩ−cm2 4H-SiC power DMOSFETs,” S. H. Ryu, S. Krishnaswami, M. Das, J. Richmond, A. Agarwal, J. Palmour, and J. Scofield, *IEEE Electron Device Lett*., Vol. 25, No. 8, pp. 556–558, 2004.
33. “10 kV 123 mΩ−cm2 4H-SiC power DMOSFETs,” S. H. Ryu, S. Krishnaswami, M. Das, J. Richmond, A.Agarwal, J. Palmour, and J. Scofield, *IEEE Electron Device Lett*., Vol. 25, No. 8, pp. 556–558, 2004.
34. “10 kV, 5A 411-SiC Power DMOSFET,” S. H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, Naples, Italy : s.n., *18th International Symposium on Power Semiconductor Devices & IC's*, 2006.
35. “On-State Characteristics of SiC power UMOSFETs on 115-µm drift Layers,” Y. Sui, T. Tsuji, J. A. Cooper, Jr., Electron Device Letters, *IEEE*, Vol. 26, No. 4, pp.255- 257, 2005.
36. http://www.grc.nasa.gov/WWW/SiC/publications/micropipeEDL/MicropipeEDLPaper.HTML
37. “Surface step model for micropipe formation in SiC,” Noboru Ohtani, Masakazu Katsuno, Tatsuo Fujimoto, Takashi Aigo, Hirokatsu Yashiro, *Journal of Crystal Growth*, Vol. 226(2), pp. 254–260, 2001.
38. “Investigation on small growth pits in 4H silicon carbide epilayers,” Xianyun Maa, Hsuehrong Changb, Qingchun Zhangb, Tangali Sudarshanc, *Journal of Crystal Growth*, Vol. 279(3–4), pp. 425–432, 2005.
39. “Vapour phase growth of epitaxial silicon carbide layers,” G. Wagner, D. Schulz, D. Siche, *Progress in Crystal Growth and Characterization of Materials*, Vol. 47(2–3), pp. 139–165, 2003.

Contact Information

Jerry Hudgins
jhudgins2@unl.edu

T: 402-472-3771

Growth pits



Reference [59]

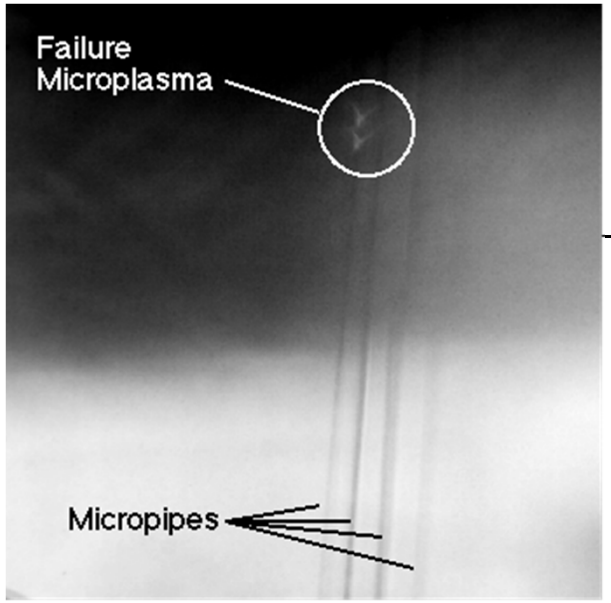
Known as surface depreciations exhibiting two morphology types:
- stripe-shaped;
- sharp-apex growth pits.

Resulting from **threading screw and edge dislocations** in 4H-SiC **epitaxial layers**.

Field enhancement may occur around the growth pints resulting in non-ideal characteristics for Schottky barrier heights of SiC devices.

Currently, the density is 1-100 cm^{-2}.

Micropipes



Reference [53]

The most prominent defect in SiC;
~~The quantity determines the wafer quality.~~

Micropipes are **super screw dislocations**, showing as holes through a wafer.

They penetrate through the entire crystal along the c-axis and have size ~ 1 μm.

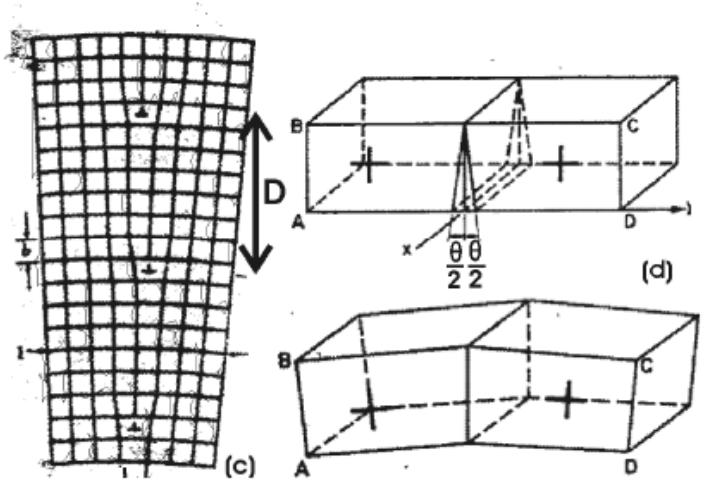
Reasons for forming:

Thermoelastic stress due to non-uniform heating;

Kinetic causes related to the nucleation process and growth surface morphology;

Technological causes depended on seed surface preparation and the growth system contamination.

Low angle boundaries (LABs)



Reference [55]

Critical defects preventing the implementation of large-size power SiC devices.

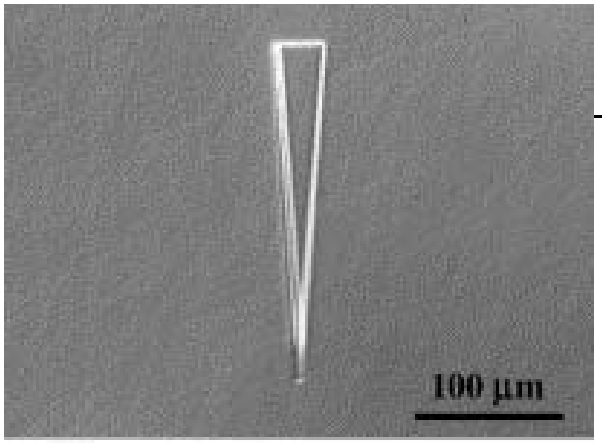
The LABs are not uniformly distributed and are due to non-optimized process condition.

The crystal periphery tends to form the growth of large diameter crystal.

The center region of a crystal generally has a better crystal quality with a lower density of LABs.

Currently, 100 mm SiC substrates are produced without LABs.

Triangular defects (TDs)



Reference [60]

TDs are isosceles triangles with varying apex angle.

TDs contain an inclusion of the 3C polytype.

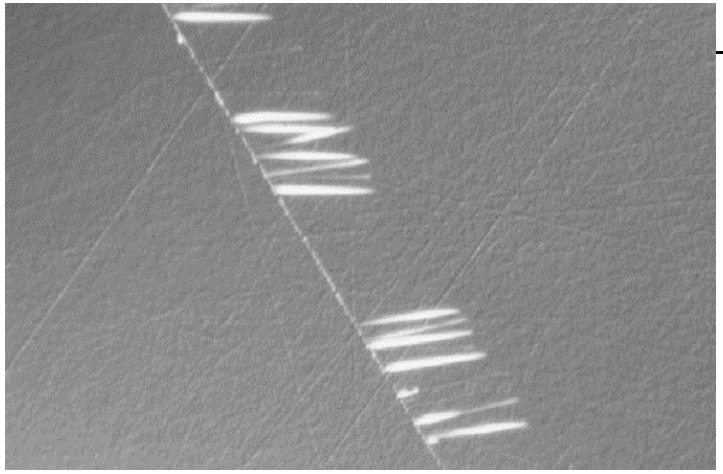
Two theory of TDs origin:

- TDs occur at substrate locations containing lattice imperfection, polishing-induced damage, or contamination;
- Formed during the step flow growth of the epitaxy. Temperature non-uniformities during epitaxial growth cause the appearance of triangle insulation of different polytypes.

TDs cause **leakage current** increasing and lowering of **breakdown voltage**.

TDs are common defects in 4H-SiC with density 1-10 cm^2.

Carrot defect (CD)



Reference [60]

CD is one of the major surface morphological defects appearing during growing of epilayers.

CDs has different shapes and structures.

CD structure consists of two stacking faults one in the prismatic plane and other in the basal plane connected through a star-rod dislocation.

Two models for CD **origin** :
Threading screw dislocations in the substrate;
Presence of foreign particle inclusion at the epi-substrate interface.

CDs - increase the leakage in pn junction, and the non-smooth surface will impact Schottky rectifying properties.

The CDs density is smaller than 5 cm^{-2}.
CD will **not be presented** in 1 cm^2 power devices in a few years.

Fowler -Nordheim (F-N) tunneling current

<u>*F-N* tunneling current - is a process in which electrons tunnel</u> through a barrier due to a high electric field.

The phenomenon is a major concern for the reliability.

$$J_{FN}(T) = A(T)\mathscr{E}_{ox}^{2} e^{\frac{-B(T)}{\mathscr{E}_{ox}}}$$

$$A(T) = \frac{q^3 m_{SiC}}{8\pi m_{ox}\Phi_b^3} \quad \text{and} \quad B(T) = \frac{4\sqrt{2m_{ox}\Phi_b^3}}{3q\hbar}$$

q - electron charge;

m_{SiC} and m_{ox} - effective electron mass in the SiC and SiO_2

$\hbar$ - reduced Planck constant

$\mathscr{E}_{ox}$ - electric field in the oxide

Φ_b - effective barrier height

$$\Phi_b = \chi - E_F(T)$$

χ - electron affinity between SiC and SiO_2

E_F - Fermi level.

SiC devices have higher *F-N* current injection compare to Si devices due to smaller barrier height.

This is a serious limitation of SiC power MOS-based devices and should be consider during design.

$$\mathscr{E}_{ox}\varepsilon_{ox} = \mathscr{E}_S\varepsilon_S$$

$$\varepsilon_{Si} > \varepsilon_{SiC}$$

For the same SiO_2 layer thickness, the electrical field in the SiC should be lower than the value used for Si. Therefore, the electrical field of the SiC material will be limited.

Replacing SiO_2 with a dielectric with bigger dielectric constant will not improve the reliability, because a material with higher dielectric constant will have smaller conduction band offset with SIC and therefore high FN tunneling current.

Schottky metal-based devices

A^{**} - modified Richardson constant;
A - area of the device;
T - operating temperature;
Φ_B - metal-semiconductor barrier height;
V_T - thermal voltage.

$$I_L = \mathbf{A}^{**} A T^2 e^{-\frac{\Phi_B}{V_T}}$$

Cree, Inc.
Schottky diodes 600 and 1700 V
MOSFET 1200 V

Infineon
Schottky barrier diodes
1200 V as discrete;
1700 V in modules.

SemiSouth
1200 and 1700 V SiC **JFETs**

Reliability of bipolar semiconductor devices

Bipolar devices (PIN diode, BJT, IGBT and thyristor) have a low V_F due to conductivity modulation in the lightly doped drift region, but the switching losses are too high.

$$\mathcal{E}_{C(SiC)} > 10 \times \mathcal{E}_{C(Si)}$$

For the same blocking voltage, SiC devices are made thinner and with higher doping concentrations of the drift region.

Storage charge is smaller and the switching losses will decrease.

Excess carrier concentration of SiC device are higher compare to Si one.

This will decrease the voltage drop in the lightly doped drift region.

n_{iSiC} is approximately 10^{20} smaller compare to n_{iSi}

$$V_{j1} = V_T \ln\left(\frac{p_{x1} N_{N^-}}{n_i^2}\right)$$

V_F >3 V and P_{ON} are high.

Limited to 150 A/cm^2, so easy dissipate heat.